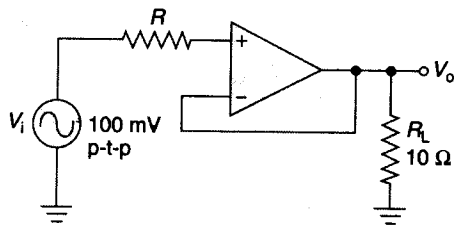


Figure 17.12 | Example 17.5.

Solution

1. Output voltage = 100 mV as the voltage gain is unity.
2. Bandwidth = Unity gain cross-over frequency = 1 MHz.
3. Load current = $(99.5 \times 10^{-3})/10 = 9.95$ mA.
4. Therefore, closed-loop output impedance = $(100 \times 10^{-3} - 99.5 \times 10^{-3})/(9.95 \times 10^{-3}) = (0.5 \times 10^{-3})/(9.95 \times 10^{-3}) = 0.05\ \Omega$.

17.4 Summing Amplifier

Summing amplifier produces an output that is equal to the sum of input signals multiplied by their corresponding voltage gain values. In the case of voltage gain being unity for all input signals, the circuit becomes an adder circuit. Again, there are inverting and non-inverting varieties of summing amplifiers. In the case of voltage gain being unity, these behave as inverting and non-inverting adder circuits.

Figure 17.13 shows circuit diagram of three input inverting-type summing amplifier. The expression for output voltage is derived as follows.

$$I_1 = \frac{V_1}{R_1},\quad I_2 = \frac{V_2}{R_2},\quad I_3 = \frac{V_3}{R_3}$$

$$I = I_1 + I_2 + I_3 = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

Also

$$I = -\frac{V_o}{R_4}$$

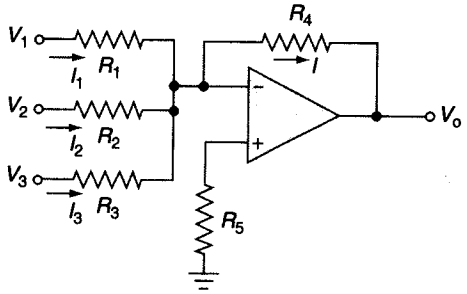


Figure 17.13 | Inverting-type summing amplifier.

Therefore

$$-\frac{V_o}{R_4}=\left(\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}\right)\Rightarrow V_o=-\left[\left(\frac{R_4}{R_1}\right)V_1+\left(\frac{R_4}{R_2}\right)V_2+\left(\frac{R_4}{R_3}\right)V_3\right] \tag{17.16}$$

If $R_1=R_2=R_3=R_4=R$, then

$$V_o=-(V_1+V_2+V_3) \tag{17.17}$$

A non-inverting summing amplifier can be constructed from its inverting counterpart by cascading it with a unity gain inverting amplifier. The complete circuit is shown in Figure 17.14. If the values of resistors R_1, R_2, R_3 and R_4 are equal and values of resistors R_6 and R_7 are also equal, then the circuit in Figure 17.14 behaves as a non-inverting adder.

Assuming $R_1=R_2=R_3=R_4=R$ and $R_6=R_7=R'$, we have

$$V_{o1}=-(V_1+V_2+V_3) \tag{17.18}$$

$$V_{o2}=-V_{o1}=V_1+V_2+V_3 \tag{17.19}$$

An alternative non-inverting adder circuit, where the summing has been done at the non-inverting input, is shown in Figure 17.15. The given circuit behaves like a non-inverting amplifier with a gain of 1 to both the inputs as is evident from the following discussion.

In the case of circuit shown in Figure 17.15, with only V_1 present and V_2 grounded, voltage V_1' at non-inverting input is given by

$$V_1'=V_1\times[(R/2)/\{R+(R/2)\}]=V_1/3 \tag{17.20}$$

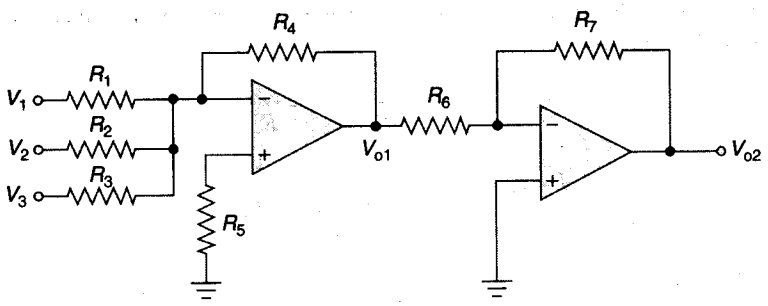


Figure 17.14 | Non-inverting type summing amplifier.

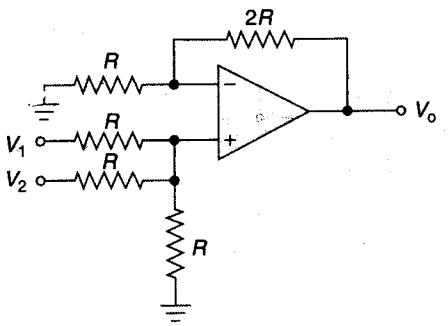


Figure 17.15 | Non-inverting adder with single opamp.

This voltage gets amplified by a gain factor $(1 + 2R/R) = 3$ to produce V_1 at the output. Similarly, with V_1 grounded, V_2 also appears as V_2 at the output. When both inputs V_1 and V_2 are simultaneously present, output is $V_1 + V_2$, that is,

$$V_o = V_1 + V_2 \tag{17.21}$$

If the adder circuit of Figure 17.15 were to be used for adding n inputs, the feedback resistor value would be equal to nR.

17.5 Difference Amplifier

Difference amplifier produces an output that is equal to the difference of the two input signals multiplied by their corresponding voltage gain values. In the case of voltage gain being unity for the two input signals, the circuit becomes a subtractor circuit. Figure 17.16 shows the generalized form of a difference amplifier. Expression for the output is derived as follows.

With V_1 grounded, output V_{o2} due to V_2 alone is given by

$$V_{o2} = V_2 \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) \tag{17.22}$$

With V_2 grounded, output V_{o1} due to V_1 alone is given by

$$V_{o1} = -V_1 \times \left(\frac{R_2}{R_1}\right) \tag{17.23}$$

When both inputs are present simultaneously, the output is equal to algebraic sum of the two. That is,

$$V_o = V_{o1} + V_{o2} = V_2 \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) - V_1 \times \left(\frac{R_2}{R_1}\right) \tag{17.24}$$

For $R_1 = R_2 = R_3 = R_4 = R$, we get

$$V_{o1} = -V_1 \text{ and } V_{o2} = V_2$$

This gives

$$V_o = V_2 - V_1 \tag{17.25}$$

Figure 17.17 shows an alternative configuration for designing a subtractor circuit. With V_2 grounded, V_1 appears as $-V_1$ at the output of first opamp and as V_1 at the output of the second opamp. With V_1 grounded, V_2 appears as $-V_2$ at the output. When both inputs are simultaneously present, output is equal to $V_1 - V_2$.

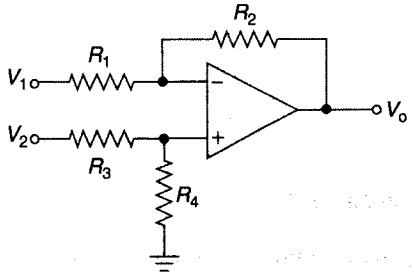


Figure 17.16 | Difference amplifier.

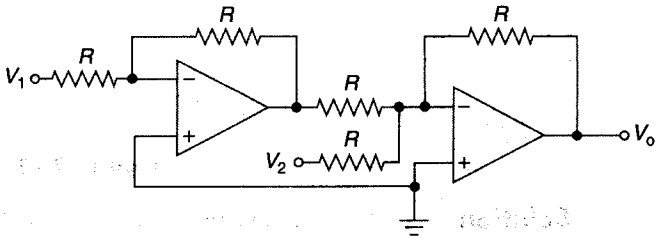


Figure 17.17 | Alternative form of subtractor circuit.

17.6 Averager

An averager circuit produces an output that is equal to the average of the amplitudes of the applied input signals. Figure 17.18 shows the generalized form of an inverting averager circuit for n inputs. The circuit configuration is similar to that of an inverting-type summing amplifier. The circuit functions as follows. With only one input present at a time and all other inputs grounded, the gain value is $-1/n$. That is, each input is multiplied by a gain value equal to $-1/n$. When all the inputs are present simultaneously, the output is given by

$$V_o = -\left[\left(\frac{V_1}{n}\right)+\left(\frac{V_2}{n}\right)+\left(\frac{V_3}{n}\right)+\cdots+\left(\frac{V_n}{n}\right)\right] \tag{17.26}$$

$$V_o = -\left(\frac{V_1+V_2+V_3+\cdots+V_n}{n}\right) \tag{17.27}$$

A non-inverting averager may be built by connecting a unity gain inverting amplifier at the output of the circuit shown in Figure 17.18.

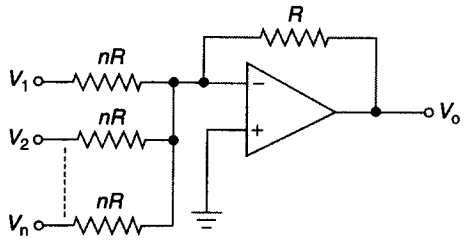


Figure 17.18 | Inverting-type averager circuit.

EXAMPLE 17.6

Refer to the summing amplifier circuit of Figure 17.19. Derive the expression for output V_o.

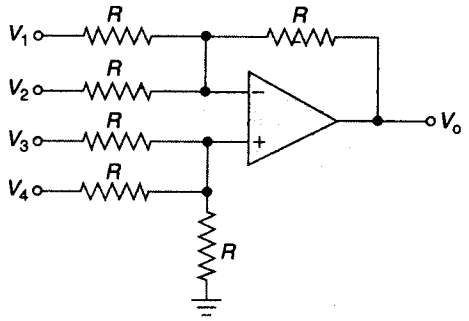


Figure 17.19 | Example 17.6.

Solution

1. Let us assume that V_{o1}, V_{o2}, V_{o3} and V_{o4} are the outputs, respectively, for V_1, V_2, V_3 and V_4 present one at a time with other inputs grounded.
2. With only V_1 present and all other inputs grounded, output $V_{o1} = -V_1$.

3. With only V_2 present and all other inputs grounded, output $V_{o2} = -V_2$.
4. With only V_3 present and all other inputs grounded, voltage appearing at non-inverting input is given by $(V_3 \times R/2)/[R + (R/2)] = V_3/3$. This gives output $V_{o3} = V_3/3 \times [1 + R/(R/2)] = V_3/3 \times 3 = V_3$.
5. Similarly, with only V_4 present and all other inputs grounded, output $V_{o4} = V_4$.
6. When all inputs are present simultaneously, output V_o equals algebraic sum of V_{o1}, V_{o2}, V_{o3} and V_{o4}.
7. That is, $V_o = V_3 + V_4 - V_2 - V_1$.

EXAMPLE 17.7

Refer to the summing amplifier circuit of Figure 17.20. Derive the expression for the output V_o.

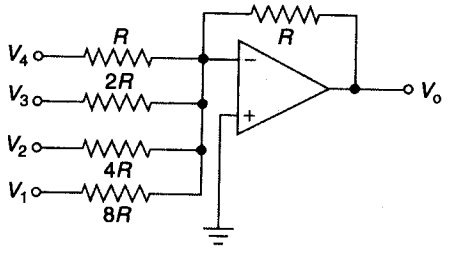


Figure 17.20 | Example 17.7.

Solution

1. Let us assume that V_{o1}, V_{o2}, V_{o3} and V_{o4} are the outputs, respectively, for only V_1, V_2, V_3 and V_4 present one at a time with other inputs grounded.
2. $V_{o4} = -V_4 \times R/R = -V_4$.
3. $V_{o3} = -V_3 \times R/2R = -V_3/2$.
4. $V_{o2} = -V_2 \times R/4R = -V_2/4$.
5. $V_{o1} = -V_1 \times R/8R = -V_1/8$.
6. With all inputs present simultaneously, $V_o = -[V_4 + V_3/2 + V_2/4 + V_1/8]$.

17.7 Integrator

An integrator circuit is the one that produces an output proportional to the integral of the input. Figure 17.21 shows the circuit diagram of the basic opamp-based integrator. Since non-inverting input terminal has been grounded, *R-C* junction is also at ground potential due to virtual earth phenomenon in opamps. Thus, the voltage V_o effectively is the voltage across the capacitor *C*.

Assuming the opamp to be ideal, due to infinite impedance at the input terminals of the opamp, current flowing through resistor *R* flows through capacitor *C* too.

$$I = \frac{V_i}{R} = -\frac{C\mathrm{d}V_o}{\mathrm{d}t}$$

so that,

$$V_o = -\frac{1}{RC}\int V_i \mathrm{d}t = K\int V_i \mathrm{d}t$$

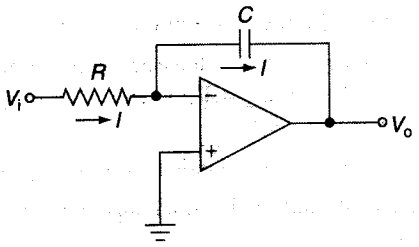


Figure 17.21 | Basic integrator.

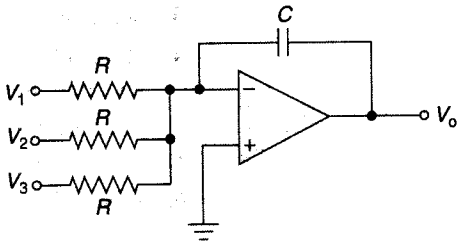


Figure 17.22 | Summing integrator.

Thus

$$V_o = K\int V_i dt \tag{17.28}$$

where $K = -1/RC$.

The basic integrator circuit suffers from DC instability problems. The circuit offers a very high gain to DC which means that even in the absence of any input, small input offset voltage might cause the output to go to positive or negative saturation. This problem can be overcome by connecting a relatively large value resistor across C. This resistor limits the DC gain to a lower value and it may be chosen to be 10 times the input resistor R. Non-inverting integrator may be built by connecting a unity gain inverting amplifier at the output of inverting integrator circuit of Figure 17.21.

Figure 17.22 shows another variation of the integrator circuit. The circuit produces an output proportional to sum of integrals of multiple inputs. That is

$$V_o = K\left(\int V_1 dt + \int V_2 dt + \int V_3 dt\right) \tag{17.29}$$

where $K = -1/RC$.

17.8 Differentiator

A differentiator circuit is the one that produces an output proportional to the differential of the input. Figure 17.23 shows the circuit diagram of the basic opamp-based differentiator. Since non-inverting input terminal has been grounded, R-C junction is also at ground potential due to virtual earth phenomenon in opamps. Thus, the voltage V_o effectively is the voltage across resistor R.

Assuming the opamp to be ideal, due to infinite impedance at the input terminals of the opamp, current flowing through resistance R flows through capacitor C too.

$$I = C\frac{dV_i}{dt} = -\frac{V_o}{R}$$

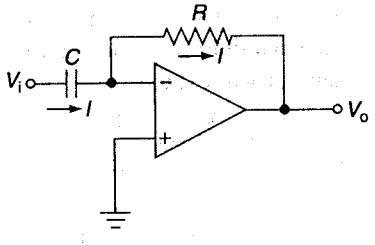


Figure 17.23 | Basic differentiator.

so that

$$V_o = -RC\frac{dV_i}{dt} \tag{17.30}$$

$$V_o = K\frac{dV_i}{dt}$$

where $K = -RC$. For $RC = 1$,

$$V_o = -\frac{dV_i}{dt}$$

Basic differentiator circuit has a tendency to go to oscillations at relatively higher frequencies. The problem can be overcome by connecting a resistor in series with the input capacitor. The resistor limits the gain at higher frequencies. The value of this resistor may be chosen to be in the range of one-tenth to one-hundredth of the feedback resistor. Non-inverting integrator may be built by connecting a unity gain inverting amplifier at the output of inverting differentiator circuit of Figure 17.23.

Figure 17.24 shows the schematic arrangement of a summing differentiator. Expression for output is derived as follows.

$$I_1 = C\frac{dV_1}{dt},\quad I_2 = C\frac{dV_2}{dt},\quad I_3 = C\frac{dV_3}{dt}$$

$$I = I_1 + I_2 + I_3 = C\left[\frac{dV_1}{dt} + \frac{dV_2}{dt} + \frac{dV_3}{dt}\right]$$

The current flowing towards inverting input terminal of the opamp is zero. This gives current through $R = I = (-V_o/R)$. This implies

$$-\frac{V_o}{R} = C\left[\frac{dV_1}{dt} + \frac{dV_2}{dt} + \frac{dV_3}{dt}\right] \tag{17.31}$$

$$V_o = -RC\left[\frac{dV_1}{dt} + \frac{dV_2}{dt} + \frac{dV_3}{dt}\right]$$

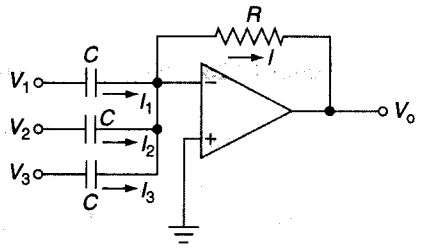


Figure 17.24 | Summing differentiator.

EXAMPLE 17.8 | *It is required to design an opamp-based circuit that generates an output V_o = (sint − cost) from the available inputs V_1 = sint and V_2 = cost. Design the circuit using (a) integrator configuration and (b) differentiator configuration.*

Solution

1. **Integrator configuration**
   - Summing integrator fed at its input by V_1 and V_2 and a unity gain inverting amplifier configuration connected at its output serves the purpose. Figure 17.25 shows the circuit diagram.
   - V_o' at the output of first opamp is given by $V_o' = -\int(V_1 + V_2)dt$ provided that $R_1C = 1$ s.
   - Final output V_o is given by $-[-\int(V_1 + V_2)dt] = \int(V_1 + V_2)dt = \int(\sin t + \cos t)dt = \sin t - \cos t$.
   - If R_1 is chosen to be equal to 10 kΩ, then for $R_1C = 1$ s, $C = 100$ μF.
   - R_2 may be taken as 10 times the value of R_1. That is, $R_2 = 100$ kΩ.
2. **Differentiator configuration**
   - Figure 17.26 shows the opamp-based differentiator circuit to implement the intended function.
   - $V_o = -\dfrac{d(V_1 + V_2)}{dt}$ provided that $R_1C = 1$ s.
   - $V_o = -\dfrac{d(\sin t + \cos t)}{dt} = \sin t - \cos t$.
   - If R_1 is chosen to be equal to 10 kΩ, then for $R_1C = 1$ s, $C = 100$ μF.
   - R_2 may be chosen to be equal to $0.01 \times R_1$. That is $R_2 = 100$ Ω.

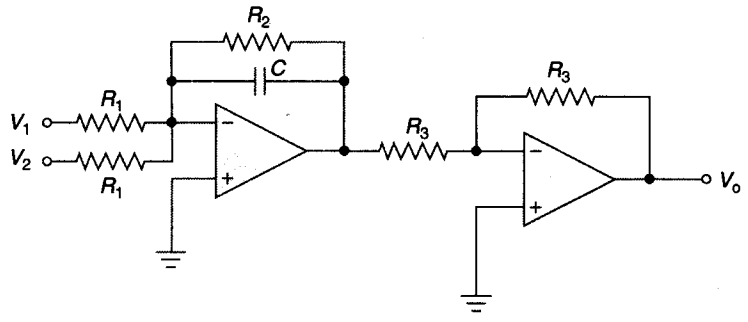


Figure 17.25 | Integrator solution for Example 17.8.

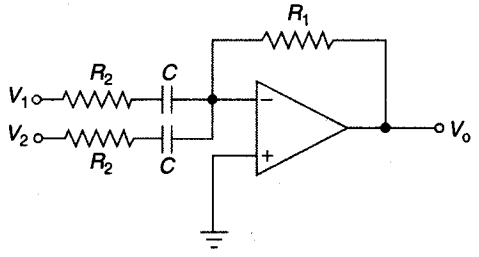


Figure 17.26 | Differentiator solution for Example 17.8.

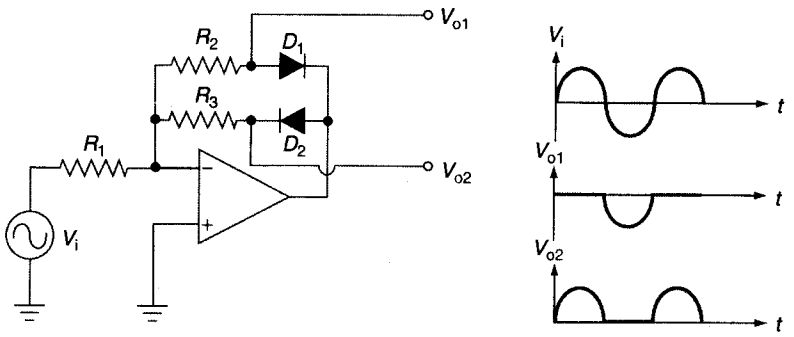


Figure 17.27 | Half-wave rectifier.

17.9 Rectifier Circuits

Conventional rectifier circuits do not produce an ideal rectified waveform at the output due to forward-biased voltage drop across the diode, which is 0.7 V in the case of silicon diodes. This problem is overcome in opamp-based rectifier circuits. Figure 17.27 shows the generalized half-wave rectifier circuit built around an opamp. The circuit functions as follows. Owing to non-inverting input of the opamp being at ground potential, during positive half cycles, diode (D_1) is forward-biased and the diode (D_2) is reverse-biased. The positive half cycles appear as negative half cycles due to phase inversion. Similarly, during negative half cycles, diode (D_1) is reverse-biased and diode (D_2) is forward-biased with the result that negative half cycles appear as positive half cycles again due to phase inversion. Remember that the moment input increases by a few milli-volts either in positive or in negative direction, the output tends to go to negative or positive saturation, respectively. It is therefore not necessary for the input to exceed the diode drop to produce the output. However, maximum values of peak positive output and peak negative output are ($V_{SAT} - 0.7$) and ($-V_{SAT} + 0.7$), respectively.

The two half-wave rectified outputs can be summed up in another opamp stage to get a full-wave rectified output as shown in Figure 17.28.

Figure 17.29 shows an alternative circuit arrangement for building a full-wave rectifier. During positive half cycle of the input signal, the diode is reverse-biased and therefore the feedback resistor is disconnected from the output of the opamp. The positive half cycles appear as such at the output. During negative half cycles, the diode is forward-biased. The negative half cycles get inverted and again appear as positive half cycles. Thus the output is a full-wave rectified signal.

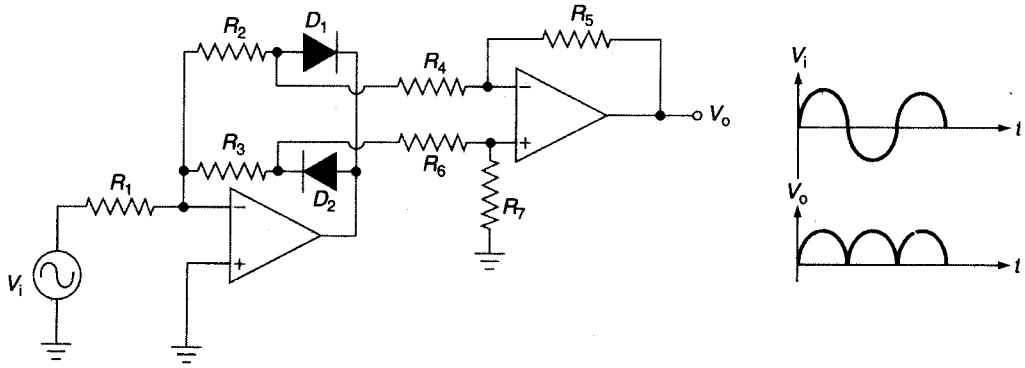


Figure 17.28 | Full-wave rectifier.

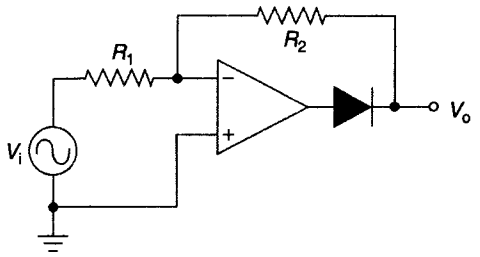


Figure 17.29 | Full-wave rectifier – alternative arrangement.

17.10 Clipper Circuits

Figure 17.30(a) shows a positive clipper circuit, a clipper circuit that clips positive half cycles above a certain reference voltage. The circuit functions as follows. During positive half cycles, for input voltages less than or equal to reference voltage (V_{REF}), the opamp output goes to positive saturation and diode (D_1) is reverse-biased with the result that the input appears as such at the output. The situation is the same during negative half cycles. When the input voltage exceeds the reference voltage (V_{REF}), the opamp output tends to go to negative saturation and the diode gets forward-biased. The output gets shorted to inverting input and the output is clamped to V_{REF}. The input and output waveforms are shown in Figure 17.30(b). If the polarity of the reference voltage is reversed in the clipper circuit of Figure 17.30(a), the clipping occurs below zero voltage as shown in Figure 17.30(b).

Figure 17.31(a) shows a negative clipper circuit. The circuit functions as follows. During positive half cycles and also for input voltages less negative or equal to $-V_{REF}$, diode D_1 is reverse-biased. The input appears as such at the output. For input voltages more negative than $-V_{REF}$, diode D_1 is forward-biased and the output gets clamped at the reference voltage. The input and output waveforms are shown in

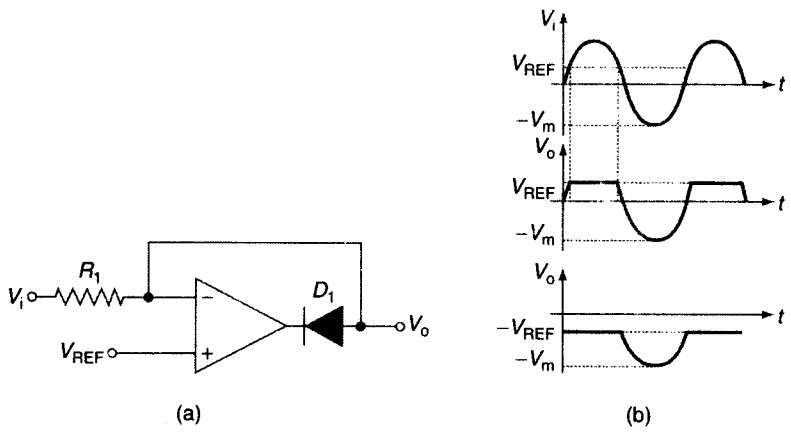


Figure 17.30 | Positive clipper circuit and relevant waveforms.

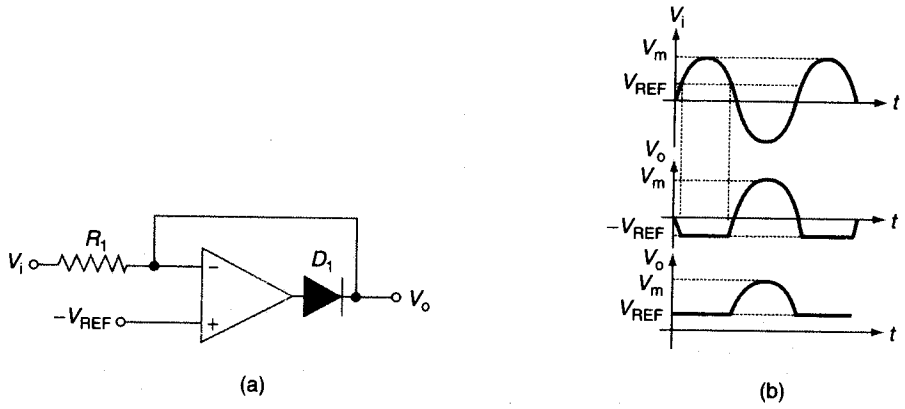


Figure 17.31 | Negative clipper circuit.

Figure 17.31(b). When the polarity of the reference voltage is reversed, clipping occurs above zero voltage. The output waveform in this case is also shown in Figure 17.31(b).

17.11 Clamper Circuits

Figure 17.32 shows the positive clamper circuit that clamps the negative peaks to zero. The circuit operates as follows. During the first negative half cycle, diode D_1 gets forward-biased and capacitor C charges through resistance R and the forward-biased diode to the peak of the negative half cycle voltage. During the positive cycle, the diode gets reverse-biased. There is no rapid discharge path for the capacitor and in this case, the output equals the input voltage plus the voltage across the capacitor. The negative peaks are thus clamped to zero voltage. If a reference voltage (V_{REF}), positive or negative, is applied to the non-inverting input terminal, the negative peaks are clamped at V_{REF} instead of zero. Figure 17.33 shows the negative clamper circuit that clamps positive peaks to zero.

The conventional clamper circuit cannot function as a clamper if the peak input signal is less than 0.7 V. The opamp-based clamper circuit has no such limitation. It functions as if the diode were ideal. This implies that the circuit can be used to clamp even milli-volt signals.

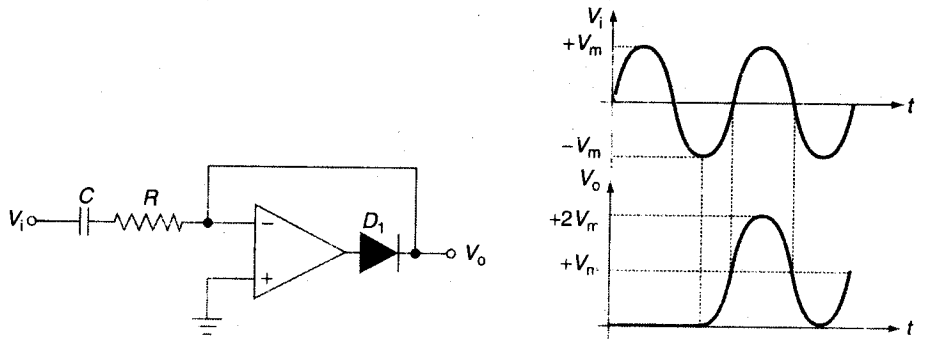


Figure 17.32 | Positive clamper circuit.

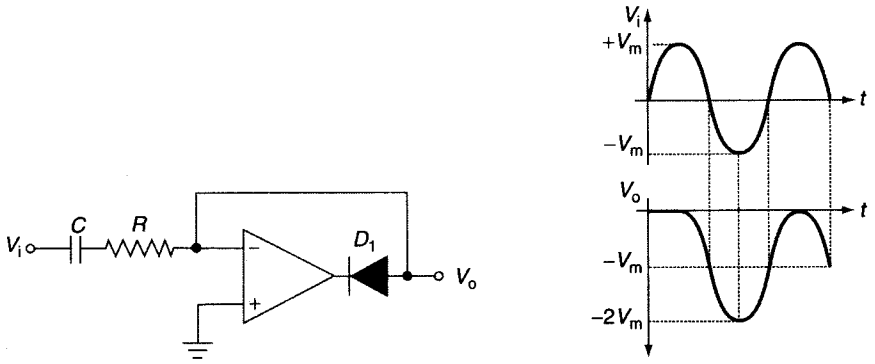


Figure 17.33 | Negative clamper circuit.

17.12 Peak Detector Circuit

Peak detector circuit produces a voltage at the output equal to peak amplitude (positive or negative) of the input signal. Figure 17.34 shows a positive peak detector circuit. As we can see, it is essentially a clipper circuit with a parallel resistor–capacitor connected at its output. The clipper here reproduces the positive half cycles. During this period, the diode D_1 is forward-biased. The capacitor rapidly charges to the positive peak from the output of the opamp through the ON resistance of the forward-biased diode. As the input starts decreasing beyond the peak, the diode gets reverse-biased, thus isolating the capacitor from the output of the opamp. The capacitor can now discharge only through the resistor (R) connected across it. The value of the resistor is much larger than the forward-biased diode's ON resistance. The purpose of this resistor is to allow a discharge path so that the output can respond to changing amplitudes of the signal peaks, decreasing amplitudes of the signal peaks to be more precise. The buffer circuit connected ahead of the capacitor prevents any discharge of the capacitor due to loading effects of the following circuit. The circuit can be made to respond to the negative peaks by reversing the polarity of the diode. Rest of the circuit is the same as in Figure 17.34.

The parallel R-C circuit time constant is typically 100 times the time period corresponding to the minimum frequency of operation. The R-C time constant also controls the response time. The response time is nothing but the time needed to respond to a decreasing peak amplitude of the input signal. Surely,

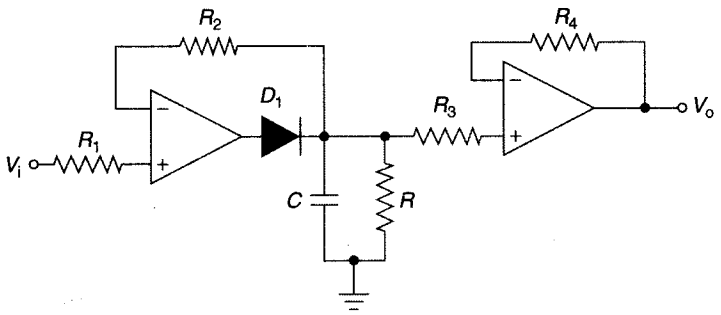


Figure 17.34 | Peak detector circuit.

a large time constant would make the response more sluggish. An attempt to reduce the time constant to improve the response time increases the output ripple. The chosen time constant is a compromise of the two conflicting requirements. Slew rate is the primary specification that needs to be looked into while choosing the right opamp for the clipper portion. The desired slew rate is such that the slew rate limited frequency, which is a function of peak-to-peak output swing and the slew rate, is at least equal to the highest frequency of operation. The peak-to-peak voltage swing at the output of the opamp is equal to $V_{pk} - (-V_{SAT}) = (V_{pk} + V_{SAT})$. Here V_{pk} is the maximum peak amplitude of the input signal and $-V_{SAT}$ is the maximum negative output voltage of the opamp.

17.13 Absolute Value Circuit

Figure 17.35 shows one possible opamp configuration that produces at its output a voltage equal to the absolute value of the input voltage. The circuit shown is a dual half-wave rectifier circuit discussed earlier followed by a difference amplifier. The circuit functions as follows.

When the applied input is of positive polarity (say $+V$), diode D_1 is forward-biased and diode D_2 is reverse-biased. The circuit reduces to what is shown in Figure 17.36. Simple mathematics shows that output (V_o) in this case is equal to $+V$. When the applied input is of negative polarity (say $-V$), diode D_1 is reverse-biased and diode D_2 is forward-biased. The equivalent circuit in this case is shown in Figure 17.37. By applying Kirchhoff's current law (KCL) at the inverting terminal of the first opamp, we can determine voltage (V_x) to be equal to $(2/3)V$. Also, V_x is related to V_o by $V_x = (2/3)V_o$. This implies that $V_o = V$. Thus the output always equals the absolute value of the input signal.

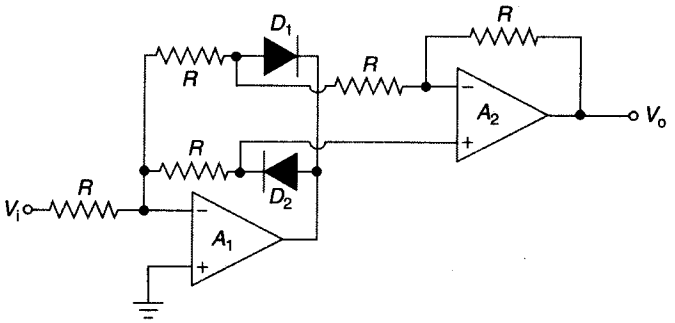


Figure 17.35 | Absolute value circuit.

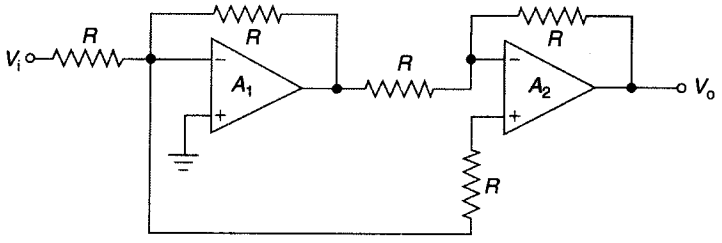


Figure 17.36 | Equivalent absolute value circuit with positive input.

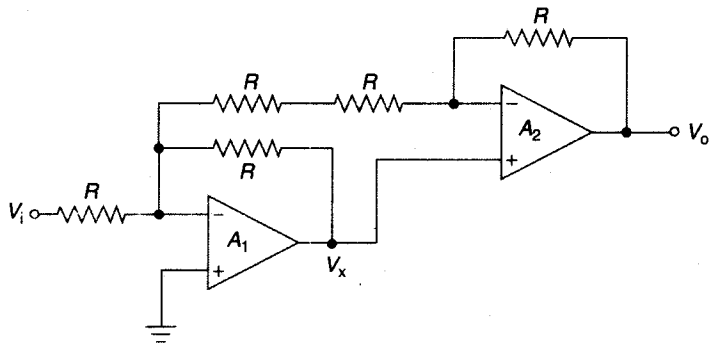


Figure 17.37 | Equivalent absolute value circuit for negative input.

17.14 Comparator

A comparator circuit is a two-input, one-output building block that produces a high or low output depending upon the relative magnitudes of the two inputs. An opamp can be very conveniently used as a comparator when used without negative feedback. Because of very large value of open-loop voltage gain, it produces either positively saturated or negatively saturated output voltage depending upon whether the amplitude of the voltage applied at the non-inverting input terminal is more or less positive than the voltage applied at the inverting input terminal.

One of the inputs of the comparator is generally applied a reference voltage and the other input is fed with the input voltage that needs to be compared with the reference voltage. In a special case where the reference voltage is zero, the circuit is referred to as zero-crossing detector. Figure 17.38 shows the basic circuit arrangement of a non-inverting type of zero-crossing detector along with its transfer characteristics. It is called a non-inverting zero-crossing detector because an input more positive than zero leads to a positively saturated output voltage. Diodes D_1 and D_2 connected at the input are to protect the sensitive input circuits inside the opamp from excessively large input voltages. Some opamps are specially designed and optimized for use as comparators. These devices have in-built protection diodes and therefore do not require external diode clamps to be connected across the input terminals. R is the current-limiting resistor.

Figure 17.39 shows the inverting type of zero-crossing detector along with its transfer characteristics. In this case, input voltage slightly more positive than zero produces a negatively saturated output voltage. One

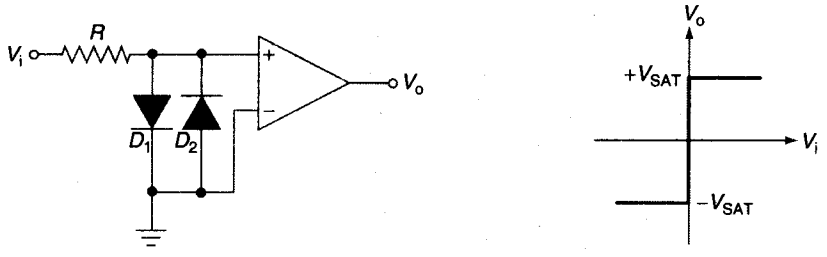


Figure 17.38 | Non-inverting zero-crossing detector.

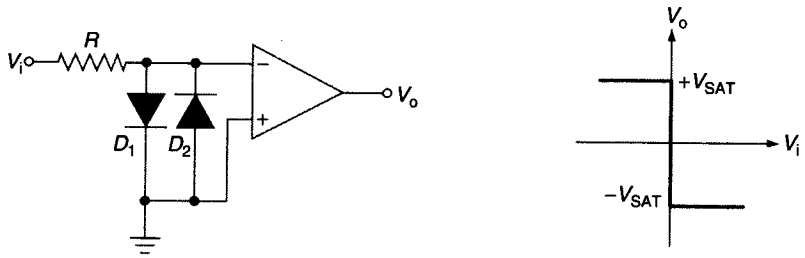


Figure 17.39 | Inverting zero-crossing detector.

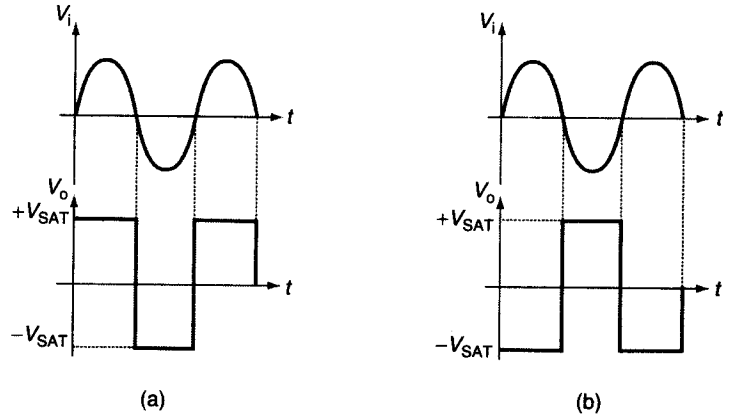


Figure 17.40 | Waveforms of (a) non-inverting zero-crossing detector; (b) inverting zero-crossing detector.

common application of zero-crossing detector is to convert sine wave signal to a square wave signal. Figures 17.40(a) and (b) respectively show relevant waveforms for non-inverting and inverting type of zero-crossing detector circuits.

In the generalized case, reference voltage may be a positive or a negative voltage. Figure 17.41 shows the circuit diagram of non-inverting comparator for a positive reference voltage. V_{REF} in this case is given by $+V_{CC} \times [R_2/(R_1 + R_2)]$. Figure 17.42 shows the circuit diagram of non-inverting comparator for a negative reference voltage. Reference voltage V_{REF} is given by $-V_{CC} \times [R_2/(R_1 + R_2)]$.

Inverting-type voltage comparators can similarly be built for positive and negative reference voltages.

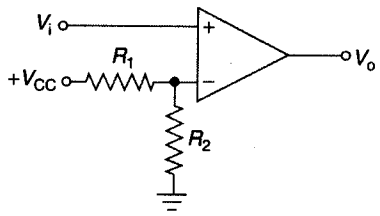


Figure 17.41 | Non-inverting comparator with positive reference.

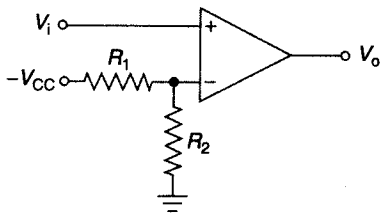


Figure 17.42 | Non-inverting comparator with negative reference.

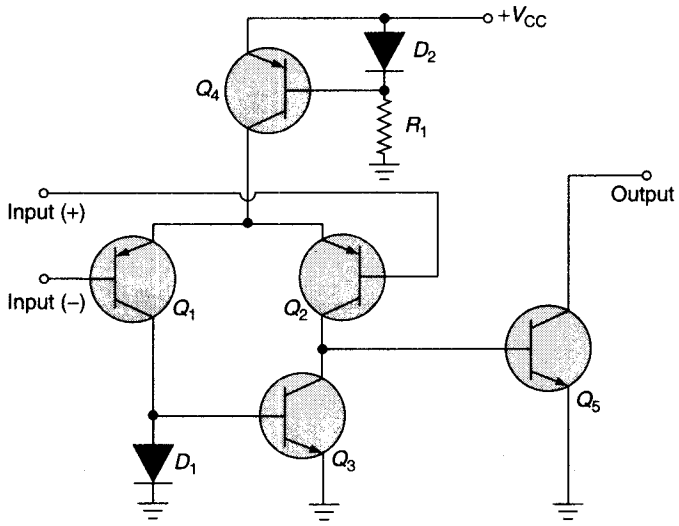


Figure 17.43 | Basic circuit schematic arrangement of opamp comparator.

Opamp Comparator

In the preceding paragraphs, we have discussed use of general-purpose opamps as voltage comparators. As outlined earlier, there are opamps that are particularly designed and optimized for use as comparators. General-purpose opamp when used as a comparator suffers from slew rate limitation. Relatively lower slew rate forces the transition time from one state to the other to be prohibitively large. Though this problem can be overcome by using a high-speed opamp with a higher slew rate specification, a better design approach to overcoming this limitation is by eliminating the compensation capacitor. It may be mentioned here that comparator works as a non-linear circuit element and therefore elimination of compensation capacitor has no derogatory effect on the performance. With compensation capacitor removed, the only capacitance remaining is the stray capacitance across the output. Thus, slew rates can be very high.

Another important parameter of a comparator is its ability to operate from a single supply and interface conveniently with popular logic families. Input circuit of opamp comparator is tailored to meet these two requirements. Figure 17.43 shows the simplified schematic diagram of opamp comparator. As seen in the figure, the output has an open-collector output stage. For the output stage to work properly, the output terminal needs to be connected to the positive supply voltage through an external resistor called pull-up resistor. It is called pull-up resistor as it pulls the output voltage to the supply voltage when the output transistor Q_5 (in Figure 17.43) is in cut-off state. Not all comparators have an open-collector output stage. In fact, pull-up resistor slows down the response time of the comparator. There are opamp comparators with active pull-up output stage that are capable of producing relatively much faster switching times. These comparators need dual power supplies.

Comparator with Hysteresis

When the input signal applied to the comparator contains noise, transitions at the output around the trip point tend to become highly erratic. Instead of being smooth from one state to the other, transition around the trip point is a cluster of pulses with randomly varying pulse width. The problem becomes particularly severe if the input signal were changing slowly. This phenomenon is demonstrated in Figure 17.44.

Figure 17.45(a) shows the circuit schematic of an inverting comparator with hysteresis along with its transfer characteristics. The circuit functions as follows. Let us assume that the output is in positive

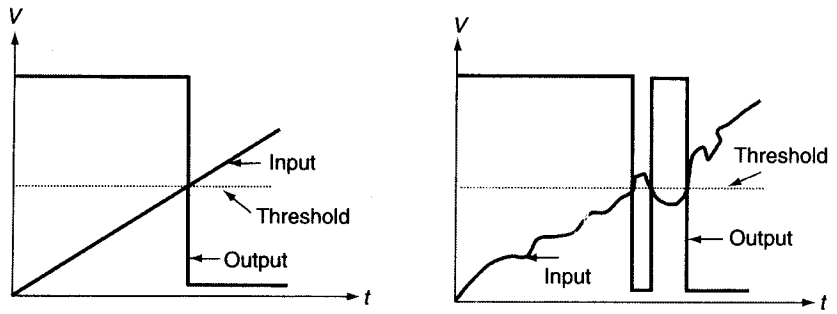


Figure 17.44 | Erratic transitions caused by noisy input signal: (a) Ideal input signal; (b) noisy input signal.

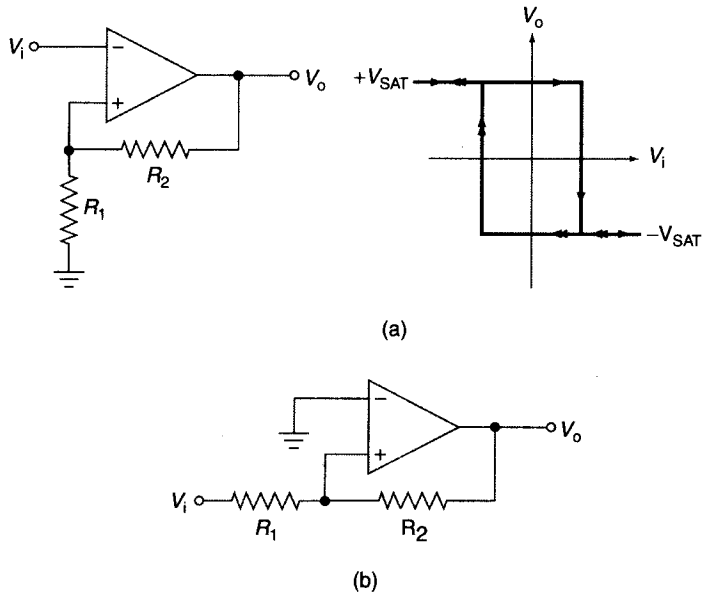


Figure 17.45 | (a) Inverting comparator with hysteresis; (b) non-inverting comparator with hysteresis.

saturation ($+V_{SAT}$). Voltage at non-inverting input in this case is $V_{SAT} \times R_1/(R_1 + R_2)$. Due to this small positive voltage at the non-inverting input, the output is reinforced to stay in positive saturation. Now, the input signal needs to be more positive than this voltage for the output to go to negative saturation. Once the output goes to negative saturation ($-V_{SAT}$), voltage fed back to non-inverting input becomes $-V_{SAT} \times R_1/(R_1 + R_2)$. A negative voltage at the non-inverting input reinforces the output to stay in negative saturation. The input signal amplitude needs to become more negative than this for the output to go to positive saturation. In this manner, the circuit offers a hysteresis of $2V_{SAT} \times R_1/(R_1 + R_2)$.

Non-inverting comparator with hysteresis can be built by applying the input signal to the non-inverting input as shown in Figure 17.45(b). Operation of the circuit can be explained on lines similar to that of its inverting counterpart. Upper and lower trip points are, respectively, given by $+V_{SAT} \times R_1/R_2$ and $-V_{SAT} \times R_1/R_2$. Hysteresis in this case is equal to $2V_{SAT} \times R_1/R_2$.

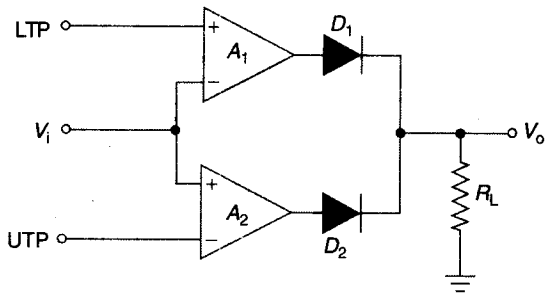


Figure 17.46 | Window comparator.

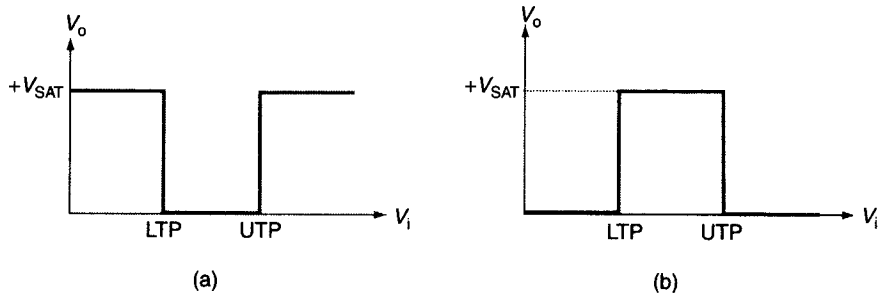


Figure 17.47 | Transfer characteristics of window comparator.

Window Comparator

In the case of a conventional comparator, the output changes state when the input voltage goes above or below the preset reference voltage. In a window comparator, there are two reference voltages called the lower and the upper trip points. Output is in one state when the input is inside the window created by the lower and upper trip points and in the other state when it is outside the window. Figure 17.46 shows the basic circuit diagram of one such window comparator. The circuit functions as follows. When the input voltage is less than the voltage reference corresponding to the lower trip point (LTP), output of opamp A_1 is at $+V_{SAT}$ and that of opamp A_2 is at $-V_{SAT}$. Diodes D_1 and D_2 are respectively forward- and reverse-biased. Consequently, output across R_L is at $+V_{SAT}$. When the input voltage is greater than the reference voltage corresponding to the upper trip point (UTP), the output of opamp A_1 is at $-V_{SAT}$ and that of opamp A_2 is at $+V_{SAT}$. Diodes D_1 and D_2 are respectively reverse- and forward-biased with the result that the output across R_L is again at $+V_{SAT}$. When the input voltage is greater than LTP voltage and lower than UTP voltage, the output of both opamps is at $-V_{SAT}$ with the result that both diodes D_1 and D_2 are reverse-biased and the output across R_L is zero.

Figure 17.47(a) shows the transfer characteristics of this window comparator. The transfer characteristics shown in Figure 17.47(b) can be obtained if we interchange the positions of LTPs and UTPs in Figure 17.46 and the comparators used are the ones with open-collector outputs. In this case a pull-up resistor will be connected from the cathode terminals of both diodes D_1 and D_2 to the supply terminal.

EXAMPLE 17.9 | *Refer to the clamping circuit of Figure 17.48. Determine the peak value of the clamped waveform at the output. Also determine the minimum recommended value of capacitance for the circuit to work as an efficient clamper. Assume the diode to be ideal.*

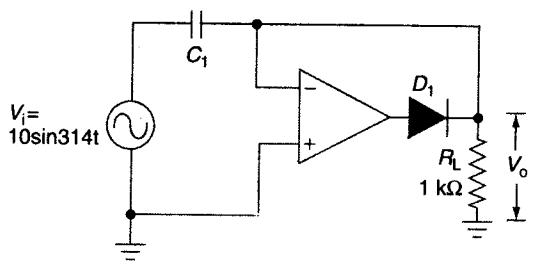


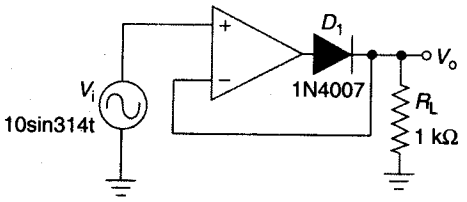
Figure 17.48 | Example 17.9.

Solution

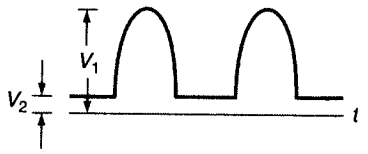
1. The given circuit clamps negative peaks of the input waveform to zero.
2. Therefore peak value of the clamped waveform = $2 \times 10 = 20$ V.
3. Frequency of input waveform = $314/2\pi = 50$ Hz.
4. This gives time period T of the input waveform as $1/50 = 20$ ms.
5. Recommended minimum value of C_1 is given by $R_L C_1 = 10T$.
6. That is, $C_1(\text{min}) = 10T/R_L = (10 \times 20 \times 10^{-3})/1000 = 200$ μF.

EXAMPLE 17.10

Refer to the half-wave circuit of Figure 17.49 and the associated rectified output waveform. Determine V_1 and V_2 given that opamp has an open-loop gain of 100 dB and diode D_1 has a cut-in voltage of 0.7 V.



(a)



(b)

Figure 17.49 | Example 17.10.

Solution

1. $V_1 = 10$ V.
2. $V_2 = 0.7/A_{OL}$, where A_{OL} is the open-loop gain of opamp.
3. $A_{OL} = 100$ dB = 100,000.
4. Therefore, $V_2 = 0.7/100{,}000 = 7$ μV.

EXAMPLE 17.11

Refer to the comparator circuit of Figure 17.50. Determine the state of LED-1 and LED-2 (whether ON or OFF) when the switch SW-1 is in (a) position-A and (b) position-B. Assume diodes D_1 and D_2 to have forward-biased voltage drop equal to 0.7 V each.

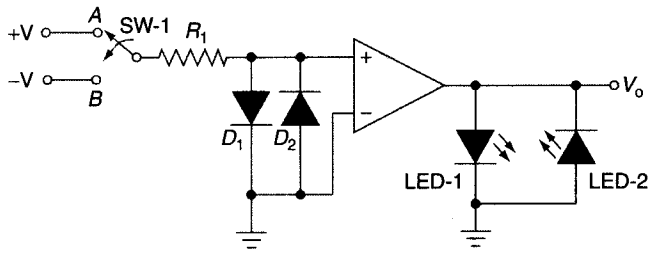


Figure 17.50 | Example 17.11.

Solution

1. When the switch SW-1 is in position-A, voltage appearing at non-inverting input is +0.7 V (equal to forward-biased voltage drop across D_1). That is, voltage at non-inverting input is more positive with respect to voltage at inverting input. Therefore, opamp output goes to positive saturation with the result that LED-1 is ON and LED-2 is OFF.
2. When the switch SW-1 is in position-B, voltage appearing at non-inverting input is –0.7 V (equal to forward-biased voltage drop across D_2). That is, voltage at non-inverting input is more negative with respect to voltage at inverting input. Therefore, opamp output goes to negative saturation with the result that LED-1 is OFF and LED-2 is ON.

EXAMPLE 17.12

Figure 17.51 shows a non-inverting type of window comparator configured around comparator IC LM 339, which is a quad comparator. Determine the lower and upper trip points of the comparator and also draw the output voltage V_o versus input voltage V_i transfer characteristics.

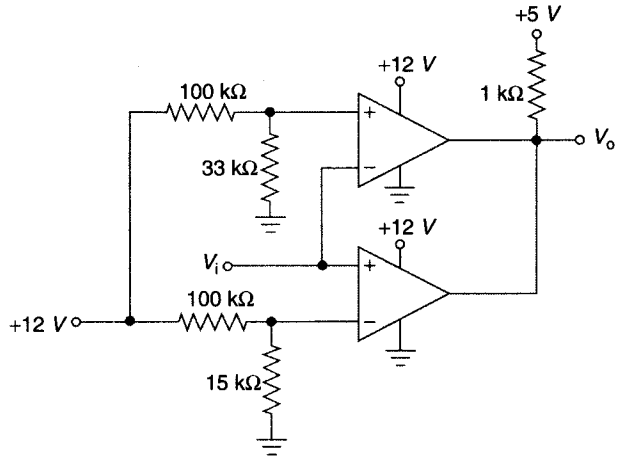


Figure 17.51 | Example 17.12.

Solution

1. Lower trip point (LTP) is given by $(12 \times 15 \times 10^3)/(115 \times 10^3) = 1.565$ V.
2. Upper trip point (UTP) is given by $(12 \times 33 \times 10^3)/(133 \times 10^3) = 2.977$ V.
3. Transfer characteristics are shown in Figure 17.52.

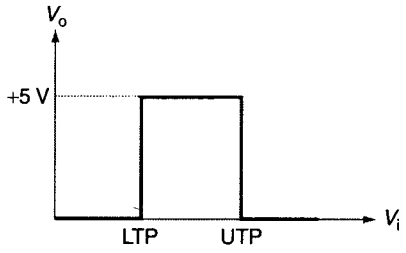


Figure 17.52 | Solution to Example 17.12.

EXAMPLE 17.13

Design an absolute value circuit using opamps to produce an output $V_o = |V_i|$ given that $-5\ V \leq V_i \leq +5\ V$ and the highest frequency likely to be encountered is 20 kHz. The circuit should have input impedance not less than 15 kΩ. Also give the desired values of slew rate and unity gain cross-over specifications of the opamp or opamps used in the circuit.

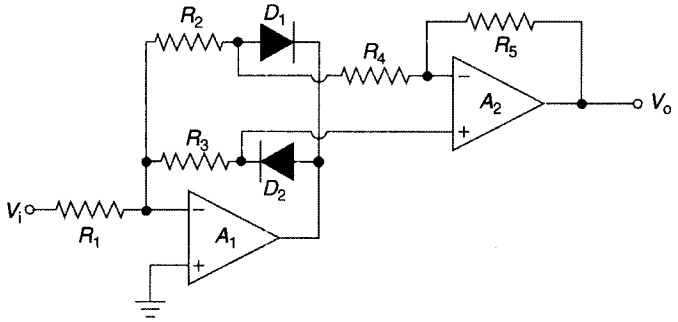


Figure 17.53 | Example 17.13.

Solution

1. Figure 17.53 shows the circuit diagram. For this circuit to produce $V_o = |V_i|$, $R_1 = R_2 = R_3 = R_4 = R_5 = R$.
2. Input impedance of this circuit equals R_1, which equals R. Therefore, $R = 15$ kΩ.
3. Peak-to-peak value of input signal = 10 V. Highest expected signal frequency = 20 kHz.
4. Therefore, required slew rate = $\pi \times f_{MAX} \times 10 = 20 \times 10^3 \times 10\pi$ V/s = 0.628 V/μs.
5. Opamps A_1 and A_2 are operating at closed-loop gain values of 1 and 1.5, respectively.
6. Therefore, unity gain cross-over frequency specifications of A_1 and A_2 should be at least 20 kHz and 30 kHz, respectively.

17.15 Active Filters

In this section we will briefly describe opamp circuits used to build low-pass, high-pass, band-pass and band-reject active filters. We will confine our discussion to first- and second-order filters. Order of an active filter is determined by number of *R-C* sections (or poles) used in the filter, which for a few exceptions equals the number of capacitors.

First-Order Filters

The simplest low-pass and high-pass active filters are constructed by connecting lag and lead type of *R-C* sections, respectively, to the non-inverting input of the opamp wired as a voltage follower. Figures 17.54(a) and (b) respectively show such first-order low-pass and high-pass filter circuits. The cut-off frequency in both cases is given by Eq. (17.32). The circuits function as follows. In the case of low-pass circuit of Figure 17.54(a), at low frequencies, reactance offered by the capacitor is much larger than the resistance value and therefore applied input signal appears at the output mostly unattenuated. At high frequencies, the capacitive reactance becomes much smaller than the resistance value thus forcing the output to be near zero. The output is 0.707 times the input when the signal frequency is such as to make the capacitive reactance equal to the resistance value. This is called the upper cut-off frequency. The gain rolls off at a rate of 6 dB per octave or 20 dB per decade beyond the cut-off point. Roll-off rate beyond the cut-off point in the case of n-order filter is $6n$ dB per octave or $20n$ dB per decade. Operation of the high-pass circuit can also be explained on similar lines.

The filters shown in Figure 17.54 can also be configured so as to have the desired amplification of the input signal. Low-pass and high-pass filter circuits with gain are shown in Figures 17.55(a) and (b), respectively. The voltage gain A_v is given by Eq. (17.33).

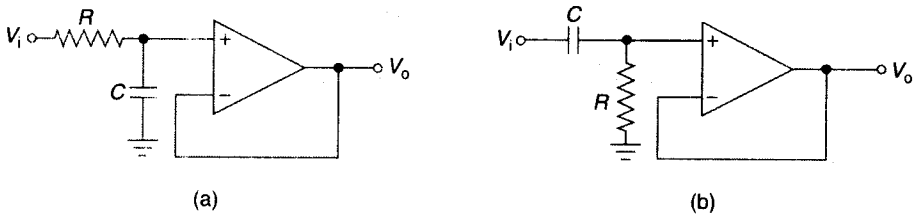
$$f_C = \frac{1}{2\pi RC} \tag{17.32}$$

$$A_v = 1 + \frac{R_3}{R_2} \tag{17.33}$$

Single-order filters shown in Figures 17.54 and 17.55 employ non-inverting type of amplifier configuration. These filters could also be implemented using inverting amplifier configuration. Relevant circuits are shown in Figures 17.56. Cut-off frequency and mid-band gain values in the case of low-pass filter are, respectively, given by Eqs. (17.34) and (17.35).

$$f_C = \frac{1}{2\pi R_2 C_1} \tag{17.34}$$

$$A_v = -\frac{R_2}{R_1} \tag{17.35}$$



(a) (b)

Figure 17.54 | First-order active filters: (a) Low pass; (b) high pass.

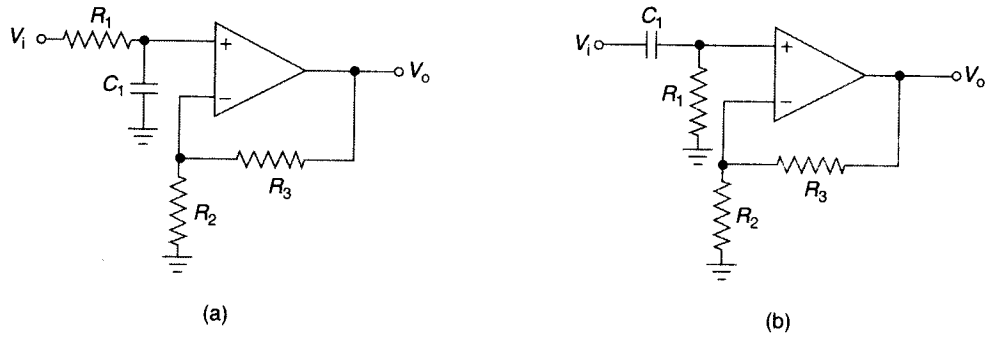


Figure 17.55 | First-order filters with gain: (a) Low pass; (b) high pass.

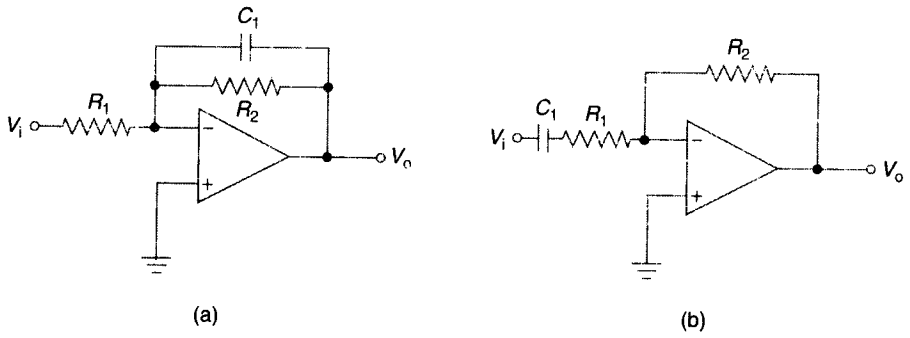


Figure 17.56 | First-order filters using inverting configuration: (a) Low pass; (b) high pass.

The same in the case of high-pass filter are given by Eqs. (17.36) and (17.37).

$$f_C = \frac{1}{2\pi R_1 C_1} \tag{17.36}$$

$$A_v = -\frac{R_2}{R_1} \tag{17.37}$$

Second-Order Filters

Figure 17.57 shows the generalized form of a second-order Butterworth active filter. Butterworth filter, also called maximally flat filter, offers a relatively flat pass and stop band response but has the disadvantage of relatively sluggish roll-off. Other commonly used filters are the Chebychev and Cauer filters. Chebychev filters offer much faster roll-off but their pass band has ripple. Cauer filters have rippled pass and stop bands. There are other types of filters such as Bessel filters with their unique properties. Discussion on all these types is beyond the scope of the present text.

In the case of generalized form of second-order Butterworth filter, shown in Figure 17.57, we have the following:

1. If $Z_1 = Z_2 = R$ and $Z_3 = Z_4 = C$, we get a second-order low-pass filter.
2. If $Z_1 = Z_2 = C$ and $Z_3 = Z_4 = R$, we get a second order high-pass filter.

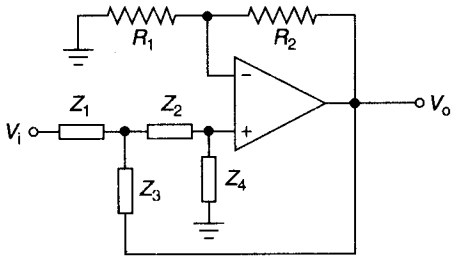


Figure 17.57 | Generalized form of second-order Butterworth filter.

The cut-off frequency is given by

$$f_C = \frac{1}{2\pi RC} \tag{17.38}$$

The value of pass band gain (A_v) can be determined from

$$A_v = 1 + \frac{R_2}{R_1} \tag{17.39}$$

Band-pass filters can be formed by cascading the high-pass and the low-pass filter sections in series. These filters are simple to design and offer large bandwidth. To construct a narrow band-pass filter, one needs to employ multiple feedback as shown in Figure 17.58. At very low frequencies, C_1 and C_2 offer very high reactance. As a result, the input signal is prevented from reaching the output. At very high frequencies, the output is shorted to the inverting input, which converts the circuit to an inverting amplifier with zero gain. Again, there is no output. Thus at both very low and very high frequencies, the output is zero. At some intermediate band of frequencies, the gain provided by the circuit offsets the loss due to the potential divider R_1–R_3. Mathematical expressions governing the design of the filter circuit are given in Eqs. (17.40)–(17.42):

Resonant frequency,

$$f_R = 2Q/2\pi R_2 C \tag{17.40}$$

where Q is the quality factor.

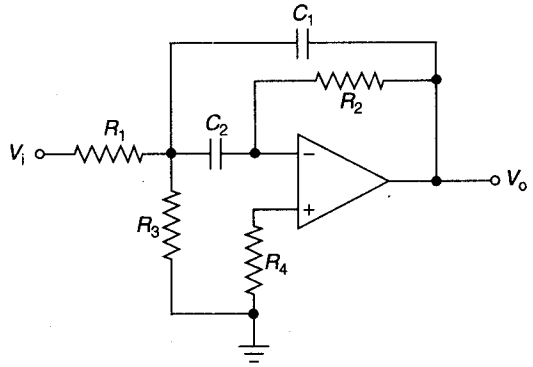


Figure 17.58 | Narrow band-pass filter.

For $C_1 = C_2 = C$, the quality factor is given by

$$Q = \left[R_1 R_2 / 2R_3\right]^{1/2} \tag{17.41}$$

The voltage gain is

$$A_v = Q/2\pi R_1 f_R C \tag{17.42}$$

Band-reject filters can be implemented by summing together the outputs of the low-pass and high-pass filters. These filters are simple to design and have a broad reject frequency range.

Figure 17.59 shows the circuit diagram of second-order narrow band reject filter. It uses a twin-T network that is connected in series with the non-inverting input of the opamp. A twin-T network offers very high reactance at the resonance frequency and very low reactance at frequencies off-resonance. This phenomenon explains the behavior of the circuit. Another way of explaining the behavior of the circuit is as follows. Very low frequency signals find their way to the output via the low-pass filter formed by R_1–R_2–C_3. Very high frequency signals reach the output through the high-pass filter constituted by C_1–C_2–R_3. In an intermediate band of frequencies, both filters pass the signal to some extent but the negative phase shift introduced by low-pass filter is cancelled out by an identical positive phase shift by high-pass filter with the result that at any instant, the net signal reaching the non-inverting input and hence the output is zero. Component values of the twin-T network are chosen according to the following equations.

$$R_1 = R_2 = R, R_3 = R/2 \tag{17.43}$$

$$C_1 = C_2 = C, C_3 = 2C \tag{17.44}$$

$$0 \le R_4 \le (R_1 + R_2) \tag{17.45}$$

$$f_R = \frac{1}{2\pi RC} \tag{17.46}$$

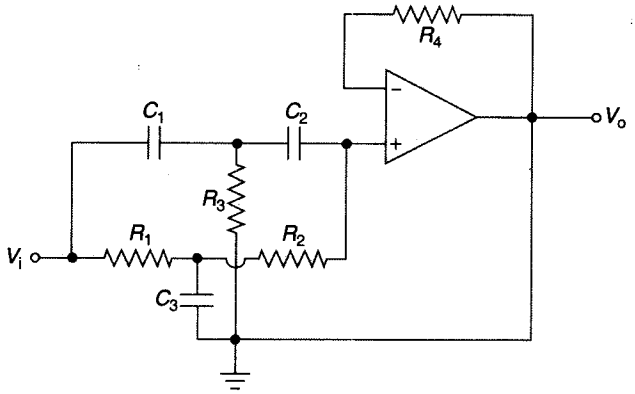


Figure 17.59 | Second-order band-reject filter.

EXAMPLE 17.14 | *Refer to the first-order low-pass filter of Figure 17.60. Determine the cut-off frequency and the gain value at four times the cut-off frequency.*

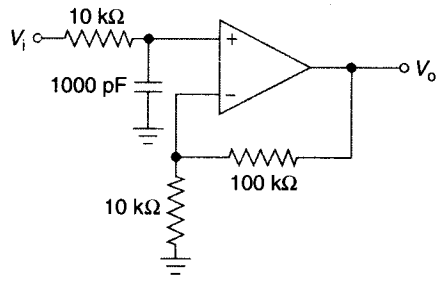


Figure 17.60 | Example 17.14.

Solution

1. Cut-off frequency,
$$f_C = 1/(2\pi \times 10 \times 10^3 \times 1000 \times 10^{-12}) = 10^5/2\pi \text{ Hz} = 15.915 \text{ kHz}$$
2. Gain, $A_v = (1 + 100 \times 10^3)/(10 \times 10^3) = 11 = 20.827$ dB.
3. Gain at cut-off point = 20.827 – 3 = 17.827 dB.
4. Gain at frequency four times the cut-off frequency will be 12 dB below the value of mid-band gain.
5. Therefore, gain at four times the cut-off frequency = 20.827 – 12 = 8.827 dB.

EXAMPLE 17.15

Figure 17.61 shows a second-order low-pass filter built around a single opamp. Calculate the values of R_1, R_2, C_1, C_2 and R_3 if the filter had a cut-off frequency of 10 kHz, Q-factor of 0.707 and input impedance not less than 10 kΩ.

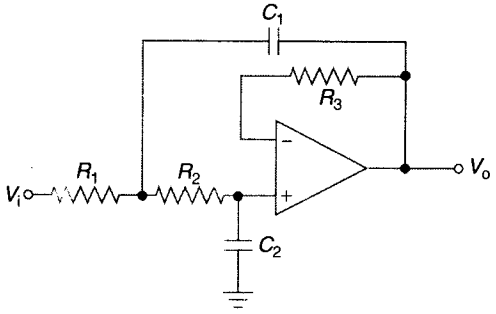


Figure 17.61 | Example 17.15.

Solution

1. For $R_1 = R_2 = R$, cut-off frequency, f_C is given by $f_C = 1/2\pi R\sqrt{C_1C_2}$.
2. Q-factor is given by $Q = (1/2) \times \sqrt{C_1/C_2}$.
3. For $Q = 0.707$, $C_1 = 2C_2$.
4. For input impedance of 10 kΩ, $R_1 = 10$ kΩ $= R_2$.
5. $f_C = 1/(2\pi \times 10 \times 10^3 \times C_2 \times \sqrt{2}) = 10 \times 10^3$.

6. This gives $C_2 = 0.0011$ μF.
7. $C_1 = 2C_2 = 0.0022$ μF.
8. R_3 is equal to $R_1 + R_2$ in order to have equal DC resistance between each opamp input and ground. Therefore, $R_3 = 20$ kΩ.

EXAMPLE 17.16

Design an opamp-based twin-T band-reject filter having a notch frequency of 100 kHz. Specify the small-signal bandwidth of the chosen opamp if the highest expected frequency were 1 MHz.

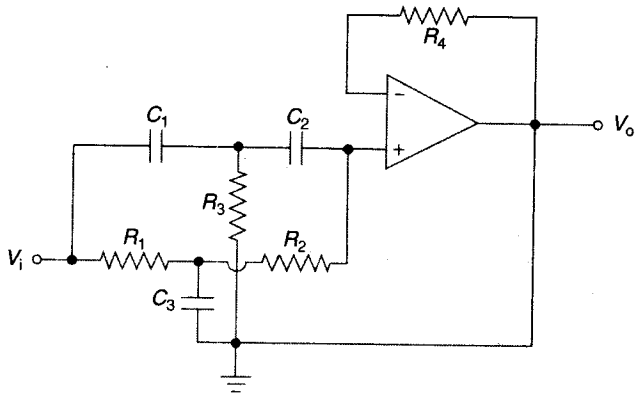


Figure 17.62 | Example 17.16.

Solution

1. Figure 17.62 shows the circuit. The notch frequency is given by $f_R = 1/2\pi RC$ where $R_1 = R_2 = R$, $C_1 = C_2 = C$, $R_3 = R/2$ and $C_3 = 2C$.
2. Let $C_1 = 0.0001$ μF. This gives $R_1 = 1/2\pi \times 100 \times 10^3 \times 0.0001 \times 10^{-6} = 15.92$ kΩ.
3. This gives $C_1 = C_2 = 0.0001$ μF and $C_3 = 0.0002$ μF.
4. $R_1 = R_2 = 15.92$ kΩ and $R_3 = 15.92 \times 10^3/2 = 7.96$ kΩ.
5. $R_4 = R_1 + R_2 = 15.92 \times 10^3 + 15.92 \times 10^3 = 31.84$ kΩ.

17.16 Phase Shifters

Figure 17.63 shows the circuit diagram of single opamp-based lagging-type phase shifter circuit. The output lags the input by an angle (θ) given by Eq. (17.47).

$$\theta \text{ (in degrees)} = -2 \tan^{-1} (\omega R_p C_p) \tag{17.47}$$

where $\omega = 2\pi f$, f being the frequency of the input signal.

The simple circuit shown in the figure can be used of shift the phase of the input signal over a wide range by varying R_p with 0° and –180° being the extremes. For $R_p << 1/\omega C_p$, the phase shift is near zero. (It will be 0° when $R_p = 0$ which is not practical). For $R_p >> 1/\omega C_p$, θ approaches –180° ($\theta = -180°$ only for $R_p =$ infinity which is again not feasible.) For $R_p = 1/\omega C_p$, $\theta = -90°$. Two such sections can be used in cascade to vary the phase shift over full 360°. Figure 17.64 shows the circuit diagram.

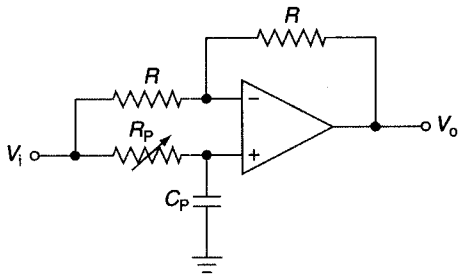


Figure 17.63 | Lagging-type phase shifter.

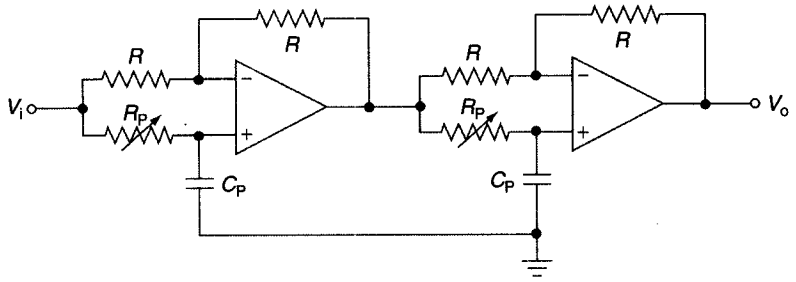


Figure 17.64 | Two-stage lagging-type phase shifter.

Figure 17.65 shows the circuit diagram of lead-type phase shifter. The circuit shown here is just the redrawn version of lagging-type phase shifter of Figure 17.63 with positions of R_p and C_p interchanged. The phase difference (θ) is given by

$$\theta \text{ (in degrees)} = 2 \tan^{-1} (\omega R_p C_p) \tag{17.48}$$

1. For $R_p = 1/\omega C_p$; $\theta = 90°$.
2. For $R_p >> 1/\omega C_p$; $\theta = 180°$.
3. For $R_p << 1/\omega C_p$; $\theta = 0°$.

Cascade arrangement of two lead-type phase shifter stages can be used for varying phase shift over full 360°.

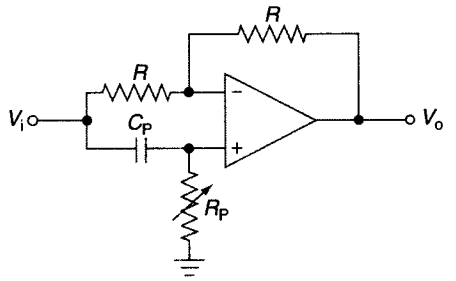


Figure 17.65 | Lead-type phase shifter.

EXAMPLE 17.17

Design an opamp-based phase shifter to shift the phase of a sine wave signal by −60° with a gain of unity. If the input signal had a peak amplitude of 5 V and the highest input signal frequency were 50 kHz, determine the slew rate of the chosen opamp.

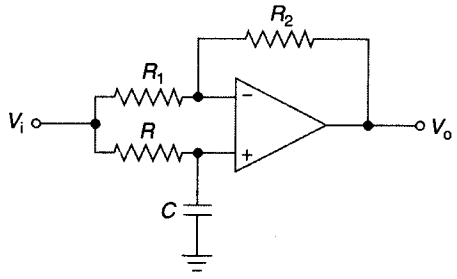


Figure 17.66 | Example 17.17.

Solution

1. Figure 17.66 shows the circuit diagram.
2. For unity gain, $R_1 = R_2$.
3. Lagging-type phase shift is given by $\theta = -2 \tan^{-1}(2\pi fRC) = -60°$.
4. This gives $2\pi fRC = \tan 30° = 0.577$.
5. Solution of above equation gives $RC = 0.184 \times 10^{-5}$.
6. Let $C = 0.001$ μF. This gives $R = (0.184 \times 10^{-5})/(0.001 \times 10^{-6}) = 1.84$ kΩ.
7. Let $R_1 = R_2 = 10$ kΩ.
8. Peak amplitude of input signal = 5 V.
9. Slew rate can be determined from f_{MAX} = Slew rate/$2\pi V_p$.
10. This gives slew rate = $2\pi \times 5 \times 50 \times 10^3 = 157 \times 10^4$ V/s = 1.57 V/μs.

17.17 Instrumentation Amplifier

Instrumentation amplifier is nothing but a differential amplifier that has been optimized for DC performance to nearly approach the DC performance of an ideal opamp. As a result, instrumentation amplifier is characterized by a high differential gain, high CMRR, high input impedance and low input offsets and low temperature drifts.

Figure 17.67 shows the classical internal schematic arrangement of an instrumentation amplifier. The two input opamps are wired as non-inverting amplifiers to provide gain and very high input impedance and the output opamp is wired as difference amplifier with unity gain. The resistors used in the output stage are ultra-high precision, low temperature drift resistors. Precision resistors with tolerance specification in the range of ±0.01% to ±0.1% and temperature drift specification of 1 PPM/°C or better are commercially available.

We will now analyze the circuit shown in Figure 17.67 for common-mode and differential-input performance. The circuit can be divided into two distinct parts, namely, the pre-amplifier stage comprising opamps A_1 and A_2 and the difference amplifier configured around A_3. Let us assume that the common-mode input is $V_{in}(CM)$. Owing to same positive voltage applied to both the non-inverting inputs, voltages appearing at the output of opamps A_1 and A_2 and also at R_1–R_2 and R_3–R_4 junctions are equal. The result is

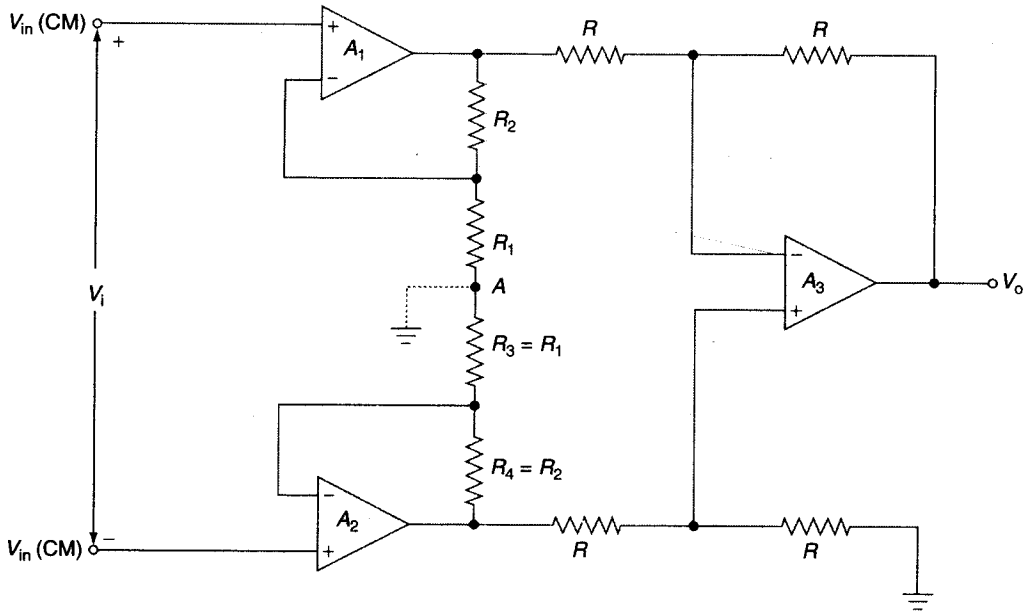


Figure 17.67 | Instrumentation amplifier.

that point A is floating. This further implies that A_1 and A_2 act like voltage followers. In other words, common-mode gain A_{CM} of the preamplifier stage is unity. Tolerance specification of R_1 and R_2 has no effect on the common-mode gain of the pre-amplifier stage.

On the other hand, when a differential signal is applied to the input, signals appearing at two R_1–R_2 and R_3–R_4 junctions are equal and opposite creating a virtual ground at point A. The differential gain of this stage is therefore $1 + (R_2/R_1)$.

The difference amplifier stage has a common-mode gain equal to $\pm 2\Delta R/R$, where ΔR represents how closely the resistors are matched. Differential gain of this stage is unity. If we combine the results, we can say that the overall common-mode gain is equal to the common-mode gain of the difference amplifier stage and overall differential gain is equal to the differential gain of the pre-amplifier stage. That is, the differential gain is given by

$$A_v = 1 + \frac{R_2}{R_1}$$

Since point A is a virtual ground and not a mechanical ground, we can use a single resistor instead of two separate resistors. If this single resistor was R_G, then $R_1 = R_3 = R_G/2$.

Therefore,

$$A_v = 1 + \frac{2R_2}{R_G} \tag{17.49}$$

The overall common-mode gain is given by

$$A_{CM} = \pm 2\Delta R/R \tag{17.50}$$

In the integrated circuit instrumentation opamps, all the components except R_G are integrated on the chip. R_G is connected externally and is used to control the voltage gain.

EXAMPLE 17.18

Refer to the instrumentation amplifier circuit of Figure 17.68. Resistors R_1 and R_2, respectively, have tolerance specifications of ±0.001% and ±0.05%. Determine the CMRR of this instrumentation amplifier in dB.

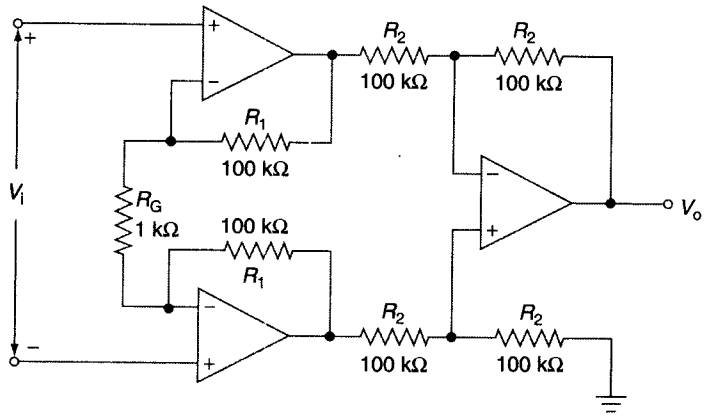


Figure 17.68 | Example 17.18.

Solution

1. Differential gain, $A_v = 1 + 2R_1/R_G$. Therefore, $A_v = 1 + [(2 \times 100 \times 10^3)/(1 \times 10^3)] = 201$.
2. Common mode gain = $\pm 2\Delta R_2/R_2 = \pm 2 \times$ Tolerance of R_2.
3. Therefore common-mode gain = $2 \times 0.0005 = 0.001$.
4. CMRR = 201/0.001 = 201000.
5. CMRR (in dB) = 20 log 201000 = 106.1 dB.

17.18 Non-Linear Amplifier

In the case of a non-linear amplifier, the gain value is a non-linear function of the amplitude of the signal applied at the input. For example, the gain may be very large for weak input signals and very small for large input signals, which implies that for a very large change in the amplitude of input signal, resultant change in amplitude of output signal is very small. A simple method to achieve non-linear amplification is by connecting a non-linear device such as a PN junction diode in the feedback path (Figure 17.69). The amplifier shown in Figure 17.69 is a semi-log amplifier as the forward current through silicon diodes varies as log of the applied voltage.

For small values of input signal, diodes act as open circuit and the gain is high due to minimum feedback. When the amplitude of input signal is large, diodes offer very small resistance and thus gain is low. Such a circuit may typically cause output voltage to change in the ratio of 2:1 for an input change of 1000:1. Resistance R_1 decides the compression ratio. Higher the value of resistor R_1, lesser is the compression ratio.

A common application of such a non-linear amplifier is in AC bridge balance detectors. The output of bridge may vary over a wide range around its null point. In order to achieve null, the output is usually

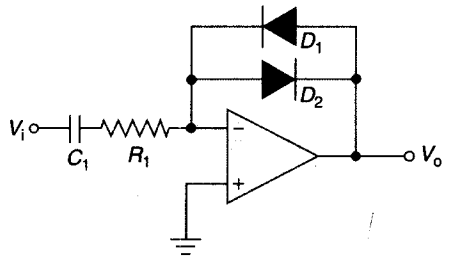


Figure 17.69 | Non-linear amplifier.

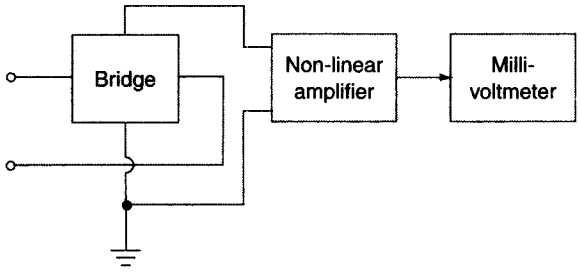


Figure 17.70 | Application of non-linear amplifier in AC bridge balance detectors.

applied to an AC milli-voltmeter whose sensitivity may have to be adjusted a number of times before a null is achieved. If the bridge output is applied to the non-linear amplifier of the type described in the preceding paragraphs (shown in Figure 17.70), the output of non-linear amplifier would vary only in a small range for a wide variation of bridge output. As an example, a variation of 10000:1 in the bridge output may cause a variation of only 6:1 in the amplifier output. This, when applied to the milli-voltmeter, enables the single range of milli-voltmeter to accommodate variations over a range of 10000:1.

17.19 Relaxation Oscillator

Relaxation oscillator is an oscillator circuit that produces a non-sinusoidal output whose time period is dependent on the charging time of a capacitor connected as a part of the oscillator circuit. Opamps adapt very well to construction of relaxation oscillator circuits that produce a rectangular output. Figure 17.71 shows the basic circuit arrangement of an opamp-based relaxation oscillator circuit.

The circuit functions as follows. Let us assume that the output is initially in positive saturation. As a result, voltage at non-inverting input of opamp is $+V_{SAT} \times R_1/(R_1 + R_2)$. This forces the output to stay in positive saturation as the capacitor C is initially in fully discharged state. Capacitor C starts charging towards $+V_{SAT}$ through R. The moment the capacitor voltage exceeds the voltage appearing at the non-inverting input, the output switches to $-V_{SAT}$. The voltage appearing at non-inverting input also changes to $-V_{SAT} \times R_1/(R_1 + R_2)$. The capacitor starts discharging and after reaching zero, it begins to discharge towards $-V_{SAT}$. Again, as soon as it becomes more negative than the negative threshold appearing at non-inverting input of the opamp, the output switches back to $+V_{SAT}$. The cycle repeats thereafter. The output is a rectangular wave. The expression for time period of output waveform can be derived from the exponential charging and discharging process and is given by

$$T = 2RC \ln\left(\frac{1+B}{1-B}\right) \tag{17.51}$$

where $B = R_1/(R_1 + R_2)$.

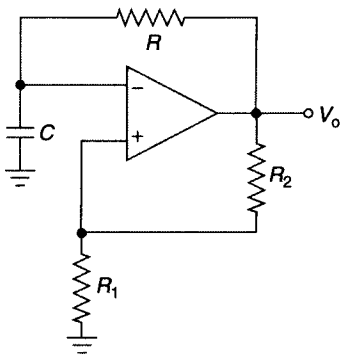


Figure 17.71 | Relaxation oscillator.

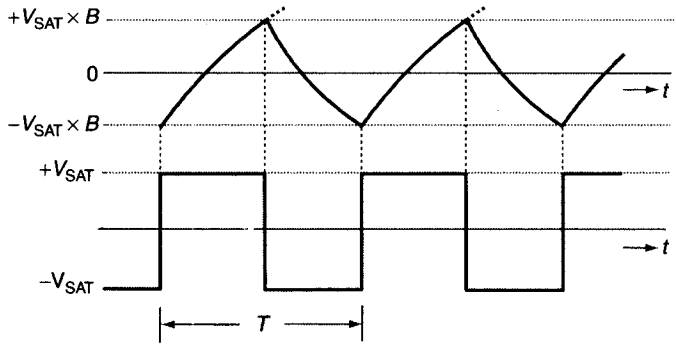


Figure 17.72 | Relevant waveforms of relaxation oscillator.

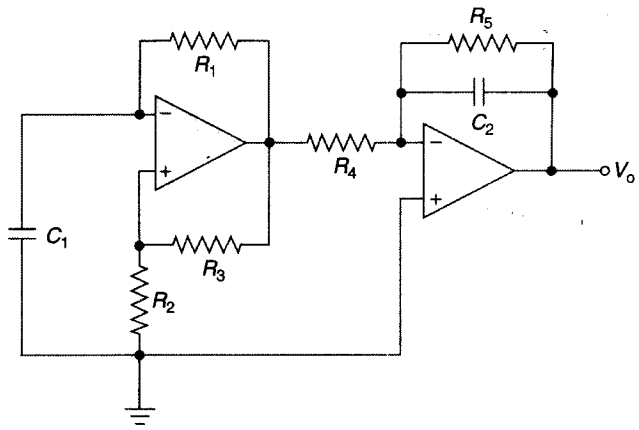


Figure 17.73 | Triangular waveform generator.

Figure 17.72 shows the relevant waveforms. The time period of output may be conveniently varied by varying the value of resistor *R*.

Relaxation oscillator forms the basis of waveform-generation circuits configured around opamps. For example, a triangular waveform generator may be built by cascading the relaxation oscillator block with an integrator block as shown in Figure 17.73.

17.20 Current-To-Voltage Converter

Current-to-voltage converter is nothing but a transimpedance amplifier. An ideal transimpedance amplifier makes a perfect current-to-voltage converter as it has zero input impedance and zero output impedance. Opamp wired as transimpedance amplifier very closely approaches a perfect current-to-voltage converter. Figure 17.74 shows the circuit arrangement. The circuit is characterized by voltage shunt feedback with a feedback factor of unity. This circuit has been discussed earlier in detail in Chapter 11 on *Negative Feedback Amplifiers*. The expressions for output voltage, closed-loop input and output impedances are given as follows.

$$V_o = I_i \times R \times \left(\frac{A_{OL}}{1 + A_{OL}} \right) \tag{17.52}$$

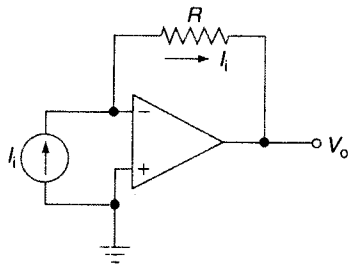


Figure 17.74 | Current-to-voltage converter.

For $A_{OL} >> 1$, Eq. (17.52) simplifies to

$$V_o = I_i \times R \tag{17.53}$$

$$Z_{in} = \frac{R}{1 + A_{OL}} \tag{17.54}$$

$$Z_o = \frac{R_o}{1 + A_{OL}} \tag{17.55}$$

where R_o is the output impedance of the opamp.

17.21 Voltage-To-Current Converter

Voltage-to-current converter is a case of a transconductance amplifier. An ideal transconductance amplifier makes a perfect voltage-controlled current source or a voltage-to-current converter. Opamp wired as transconductance amplifier very closely approaches a perfect voltage-to-current converter. Figure 17.75 shows the basic circuit arrangement. The circuit is characterized by current series feedback. This circuit has been discussed earlier in detail in Chapter 11 on *Negative Feedback Amplifiers*. Expressions for output current, closed-loop input and output impedances are given as follows.

$$I_o = \frac{V_i}{R_1 + [(R_1 + R_2)/A_{OL}]} \tag{17.56}$$

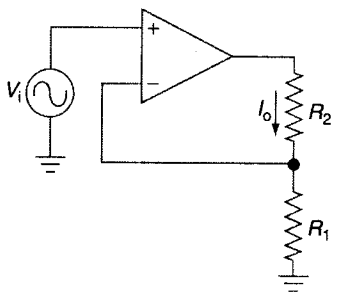


Figure 17.75 | Voltage-to-current converter.

For $A_{OL} >> 1$, Eq. (17.56) simplifies to the following equation:

$$I_o = \frac{V_i}{R_1} \tag{17.57}$$

Closed-loop input impedance is given by

$$Z_{in} = R_i \times \left(1 + A_{OL} \times \frac{R_1}{R_1 + R_2}\right) \tag{17.58}$$

where R_i is the input impedance of the opamp.

Closed-loop output impedance is given by

$$Z_o = R_1 \times \left(1 + A_{OL} \times \frac{R_1}{R_1 + R_2}\right) \tag{17.59}$$

Voltage-to-current converter of Figure 17.75 operates with a floating load, which is not always convenient. Monolithic opamps specially designed as transconductance amplifiers to feed single-ended load resistances are commercially available.

EXAMPLE 17.19

Refer to the relaxation oscillator circuit of Figure 17.76. Determine the peak-to-peak amplitude and frequency of the square wave output given that saturation output voltage of the opamp is ±12.5 V at power supply voltages of ±15 V.

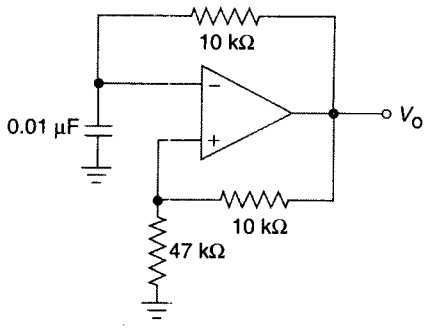


Figure 17.76 | Example 17.19.

Solution

1. The feedback factor B is given by $(47 \times 10^3)/(47 \times 10^3 + 10 \times 10^3) = 0.825$.
2. Time period T of the output waveform is given by $T = 2RC \ln [(1 + B)/(1 - B)]$.
3. That is, $T = 2 \times 10 \times 10^3 \times 0.01 \times 10^{-6} \times \ln[(1 + 0.825)/(1 - 0.825)] = 0.469$ ms.
4. Therefore, $f = 1/0.469$ kHz $= 2.13$ kHz.
5. Peak-to-peak amplitude of output $= 2V_{SAT} = 25$ V.

EXAMPLE 17.20

For current-to-voltage converter circuit of Figure 17.77, determine output voltage, closed-loop input and output impedances given that chosen opamp has open-loop transimpedance gain of 100,000, input impedance of 1 MΩ and output impedance of 100 Ω.

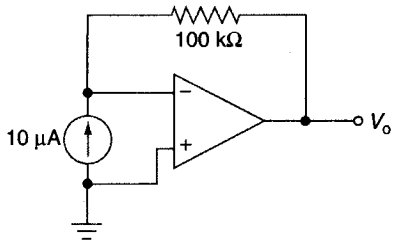


Figure 17.77 | Example 17.20.

Solution

1. Output voltage = $10 \times 10^{-6} \times 100 \times 10^3 = 1$ V.
2. Closed-loop input impedance, $Z_{in} = R/(1 + A_{OL}) = 100 \times 10^3/(1 + 100{,}000) = 1\ \Omega$.
3. Closed-loop output impedance, $Z_o = R_o/(1 + A_{OL}) = 100/(1 + 100{,}000) = 0.001\ \Omega$.

17.22 Sine Wave Oscillators

Opamps adapt well to use in building sine wave oscillators, for example, in building RC oscillators – such as RC phase shift oscillator, Wien bridge oscillator and LC oscillators – such as Hartley, Colpitt and Clapp oscillators. Opamp-based sine wave oscillators are discussed in detail with large number of solved examples in Chapter 12 on *Sinusoidal Oscillators*.

KEY TERMS

Absolute value circuit
Active filter
Averager
Comparator
Current-to-voltage converter
Difference amplifier
Differentiator
Instrumentation amplifier
Integrator
Inverting amplifier
Non-inverting amplifier
Non-linear amplifier
Peak detector circuit
Phase shifter
Relaxation oscillator
Summing amplifier
Voltage follower
Voltage-to-current converter
Window comparator

OBJECTIVE-TYPE EXERCISES

Multiple-Choice Questions

1. Magnitude of closed-loop voltage gain of inverting amplifier is given by
   a. ratio of feedback resistance to input resistance.
   b. ratio of input resistance to feedback resistance.
   c. ratio of sum of input and feedback resistances to input resistance.

d. ratio of sum of input and feedback resistances to feedback resistance.

2. Magnitude of closed loop voltage gain of non-inverting amplifier is given by
   a. ratio of feedback resistance to the resistance connected from inverting input to ground.
   b. ratio of resistance connected from inverting input to ground to feedback resistance.
   c. ratio of sum of resistance connected from inverting input to ground and feedback resistance to resistance connected from inverting input to ground.
   d. none of these.

3. In a non-inverting amplifier, when the feedback resistance equals the resistance connected from inverting input to ground, the closed-loop gain is
   a. 1.
   b. 2.
   c. Infinity.
   d. less than 1.

4. In order to construct a voltage follower,
   a. input is applied to inverting input and the non-inverting input is shorted to output.
   b. input is applied to non-inverting input and inverting input is grounded.
   c. input is applied to inverting input and non-inverting input is grounded.
   d. input is applied to non-inverting input and the inverting input is shorted to output.

5. In an opamp circuit, "*N*" DC inputs are connected to the inverting input through individual resistances, which are of the same value. The feedback resistance connected from output to inverting input is of resistance value that is 1/*N*th of the input resistance value. Non-inverting input is grounded. The output in this case is
   a. indeterminate from given data.
   b. average of all inputs.
   c. sum of all inputs.
   d. none of these.

6. The roll-off rate in fourth order Butterworth low pass filter will be
   a. 80 dB per decade.
   b. 80 dB per octave.
   c. 24 dB per decade.
   d. 12 dB per octave.

7. If the input to an integrator were a rectangular pulse, the output would be
   a. sine wave.
   b. ramp.
   c. rectangular pulse.
   d. cosine wave.

8. Output of a relaxation oscillator circuit is a
   a. sine wave.
   b. cosine wave.
   c. square wave.
   d. triangular wave.

9. Cascade arrangement of relaxation oscillator and an integrator makes a
   a. triangular waveform generator.
   b. square waveform generator.
   c. sawtooth waveform generator.
   d. pulse generator.

10. Introduction of hysteresis in a comparator makes it
    a. prone to false triggering caused by noisy input signal.
    b. immune to false triggering caused by noisy input signal.
    c. a square waveform generator.
    d. none of these.

11. In an inverting summer circuit using opamp, DC voltages of +1 V, −2 V and +2 V are, respectively, applied to the input through 10 kΩ, 20 kΩ and 50 kΩ resistors. If the feedback resistance were 50 kΩ, the output voltage would then be
    a. +2 V
    b. −2 V
    c. −3 V
    d. +3 V

12. Figure 17.78 shows transfer characteristics of some opamp circuit. It could possibly be
    a. an inverting comparator.
    b. a non-inverting comparator.

c. an inverting amplifier with hysteresis.
d. a non-inverting amplifier with hysteresis.

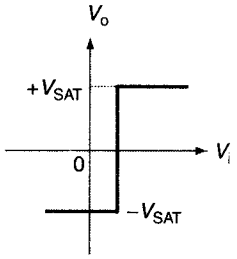


Figure 17.78 | Question 12.

13. Refer to the transfer characteristics shown in Figure 17.79. Identify the circuit.

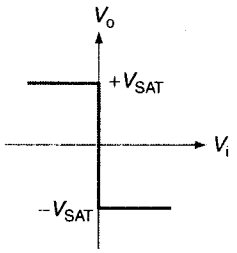


Figure 17.79 | Question 13.

a. Inverting comparator
b. Non-inverting comparator
c. Inverting zero-crossing detector
d. Non-inverting zero-crossing detector

14. Figure 17.80 shows opamp-based integrator circuit. If this circuit were to integrate a symmetrical pulse waveform of 200 μs time period and if the DC gain of the integrator were to be limited to 100, what would be the values of C_1 and R_2?

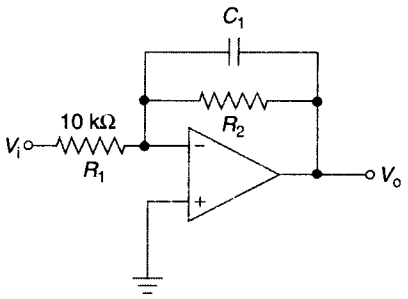


Figure 17.80 | Question 14.

a. 0.1 μF, 1 MΩ
b. 0.01 μF, 1 MΩ
c. 0.1 μF, 100 kΩ
d. 0.01 μF, 100 kΩ

15. Refer to the opamp circuit of Figure 17.81. The circuit performs the function of which important building block.

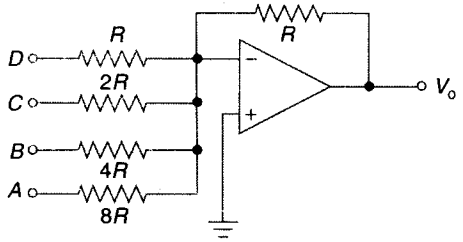


Figure 17.81 | Question 15.

a. 4-input inverting summer
b. 4-input inverting averager
c. 4-bit D/A converter
d. Multiple input inverting amplifier

REVIEW QUESTIONS

1. With the help of circuit diagram, briefly describe the operation of an inverting amplifier. Derive expressions for voltage gain, input impedance and output impedance.
2. When an opamp is used in amplifier (inverting or non-inverting) configuration, what decides the maximum operational frequency for a given value of voltage gain? How is maximum operational frequency related to various relevant parameters in the case of a sine wave input signal?
3. On what parameters does the input impedance in the case of following opamp-based circuits depend upon:
   a. Inverting amplifier
   b. Non-inverting amplifier
   c. Current-to-voltage converter
   d. Voltage-to-current converter
   e. Instrumentation amplifier

4. Give a suitable circuit diagram that can be used to subtract two DC voltages. Derive an expression to prove that the output is difference of the two inputs.
5. Draw the circuit diagram of a voltage follower. What are its closed-loop voltage gain and bandwidth?
6. Draw the basic circuit schematic of a classical three-opamp instrumentation amplifier. Briefly describe its operational principle with particular reference to the role of the two opamps constituting the input stage and the output opamp wired as differential amplifier.
7. What is the main advantage of using an opamp-based rectifier over conventional rectifier? With the help of relevant circuit schematics, explain the functional principle of (a) half-wave rectifier that clips positive half cycles and (b) peak detector.
8. What is an absolute value circuit? Draw the circuit schematic of one such circuit configured around opamp and briefly describe its functional principle.
9. Draw the circuit diagram of (a) phase shifter circuit that can introduce a phase shift in the range of 0° to −150° in a sine wave input signal and (b) phase shifter circuit that can introduce a phase shift of 0° to +150° in a sine wave input signal.
10. What is the main advantage of using a comparator with hysteresis over a conventional comparator? Explain with the help of relevant transfer characteristics.
11. With the help of relevant circuit schematic of a non-inverting comparator with hysteresis, briefly describe its operation and draw its transfer characteristics.
12. What is a window comparator? Draw the circuit diagram of a window comparator that produces a high output for input signal inside the window and a low output for input outside the window.
13. Draw the circuit schematic of a suitable opamp-based circuit that can be used to convert input sine wave signal into a symmetrical square wave output and briefly describe its operation.
14. Draw the circuit diagram of a current-to-voltage converter using opamp. What type of feedback is used in this circuit? What decides the maximum value of feedback resistance to be used in the circuit?
15. Give a suitable circuit schematic for building a triangular waveform generator using opamps. Briefly describe its operation.

PROBLEMS

1. You are asked to choose an appropriate opamp type number for your inverting amplifier configuration that has been designed for a voltage gain of 10. The input is a sinusoidal signal with peak-to-peak amplitude of 2 V. If the highest expected input signal frequency is 50 kHz, what should be the slew rate of the chosen opamp?
2. Design an opamp-based current to voltage converter having a transresistance gain of 100,000.
3. Design a non-inverting zero-crossing detector with a hysteresis of 100 mV. If the opamp had output saturation voltages of ±10 V, determine the highest input frequency that would yield output waveform transition time of not more than 10% of half of the time period of input signal. Chosen opamp has slew rate of 10 V/μs.
4. Refer to the comparator circuit of Figure 17.82. Determine the duty cycle of the output waveform.

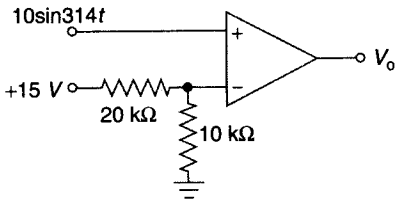


Figure 17.82 | Problem 4.

5. Figure 17.83 shows an inverting comparator with in-built hysteresis. Determine the peak-to-peak noise voltage that the comparator can withstand without false triggering given that LM 741 produces positive and negative saturation output of ±11 V for a power supply voltage of ±12 V.

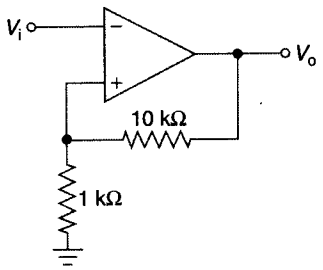


Figure 17.83 | Problem 5.

6. Refer to the opamp circuit of Figure 17.84. Identify the circuit and determine the output voltage.

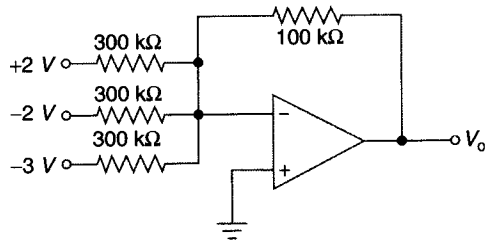


Figure 17.84 | Problem 6.

7. Determine the expression for the output voltage for the differentiator circuit of Figure 17.85.

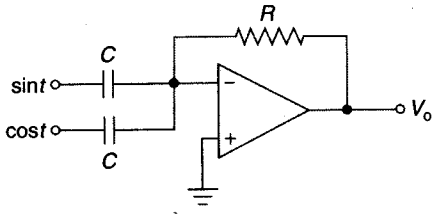


Figure 17.85 | Problem 7.

8. Identify the active filter circuit of Figure 17.86. Determine the cut-off frequency and voltage gain to DC.

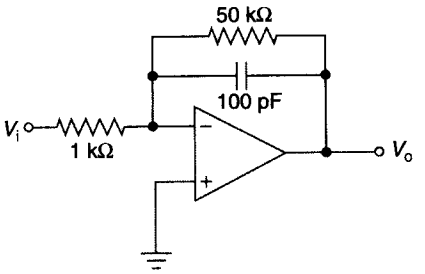


Figure 17.86 | Problem 8.

ANSWERS

Multiple-Choice Questions

1. (a)	4. (d)	7. (b)	10. (b)	13. (c)
2. (c)	5. (b)	8. (c)	11. (b)	14. (a)
3. (b)	6. (a)	9. (a)	12. (b)	15. (c)

Problems

1. 3.14 V/μs
2. Figure 17.87

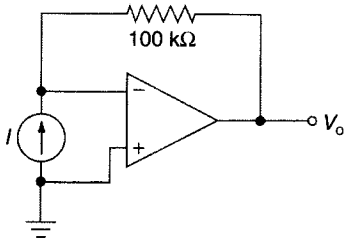


Figure 17.87 | Solution to Problem 2.

3. Figure 17.88 with $R_2/R_1 = 199$, $f_{MAX} = 25$ kHz

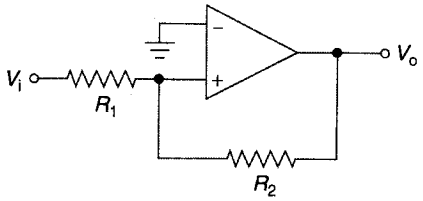


Figure 17.88 | Solution to Problem 3.

4. 1/3
5. 2 V
6. Averager, 1 V
7. $\sin t - \cos t$
8. Low-pass filter, 31.84 kHz, 50

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